EPSON
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S2R72A4x Series
Data Sheet

S2R72A44F12C4
S2R72A43F12C4
S2R72A42F12C4
S2R72A44F07E2
S2R72A43F07E2
S2R72A42F07E2

SEIKO EPSON CORPORATION

Rev.1.40

NOTICE

Table of Contents

1. Overview

The S2R72A44F12C4, S2R72A43F12C4, S2R72A42F12C4, S2R72A44F07E2, S2R72A43F07E2 and S2R72A42F07E2 are USB hub controller LSIs supporting USB 2.0 (Universal Serial Bus Specification Revision 2.0) high-speed mode. They meet the stringent quality requirements for automotive use and are capable of operating at temperatures up to 105°C.

All LSIs in the range feature two downstream ports supporting high-speed mode, while the number of downstream ports supporting full-speed mode varies for individual LSI types.

Using the A44, A43 or A42 enables the main chip USB host port to be easily expanded to allow the connection of multiple USB devices such as mobile audio players or ETC devices to car navigation systems.

2. Features

- **Wide temperature range**

  Operating temperature range is -40°C to +105°C.

- **Low power consumption**

  Low power consumption is achieved using the power management function.

- **USB specifications**

  Upstream port

  Supports HS (480 Mbps) and FS (12 Mbps) (automatic detection).

  Built-in termination (no external resistor required).

  Supports USB 1.1 mode operating as FS-HUB.

  Downstream ports

  S2R72A44: 4 ports (HS compatible port x 2, FS compatible port x 2)

  S2R72A43: 3 ports (HS compatible port x 2, FS compatible port x 1)

  S2R72A42: 2 ports (HS compatible port x 2)

  HS compatible ports support HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps).

  FS compatible ports support FS (12 Mbps) and LS (1.5 Mbps).

  All ports have built-in termination (no external resistor required).

  Built-in single transaction translator with four non-periodic buffers.

  Supports Gang or Individual (overcurrent control).

  Upstream port pin (U0_DP/U0_DM) configuration enabling straight connection to main chip.

- **Other specifications**

  Supports 12 MHz crystal oscillator (with built-in oscillator circuit and feedback resistor).

  Power supply voltage: USB power supply 3.3 V, internal core voltage 1.8 V

  Package: **QFP package (48-pin, 7 mm square, 0.5 mm pitch, 1.4 mm thickness)**
  S2R72AxF12C4 series
  SQFN package (48-pin, 7 mm square, 0.5 mm pitch, 1.0 mm thickness)
  S2R72AxF07E2 series

3. Block Diagram

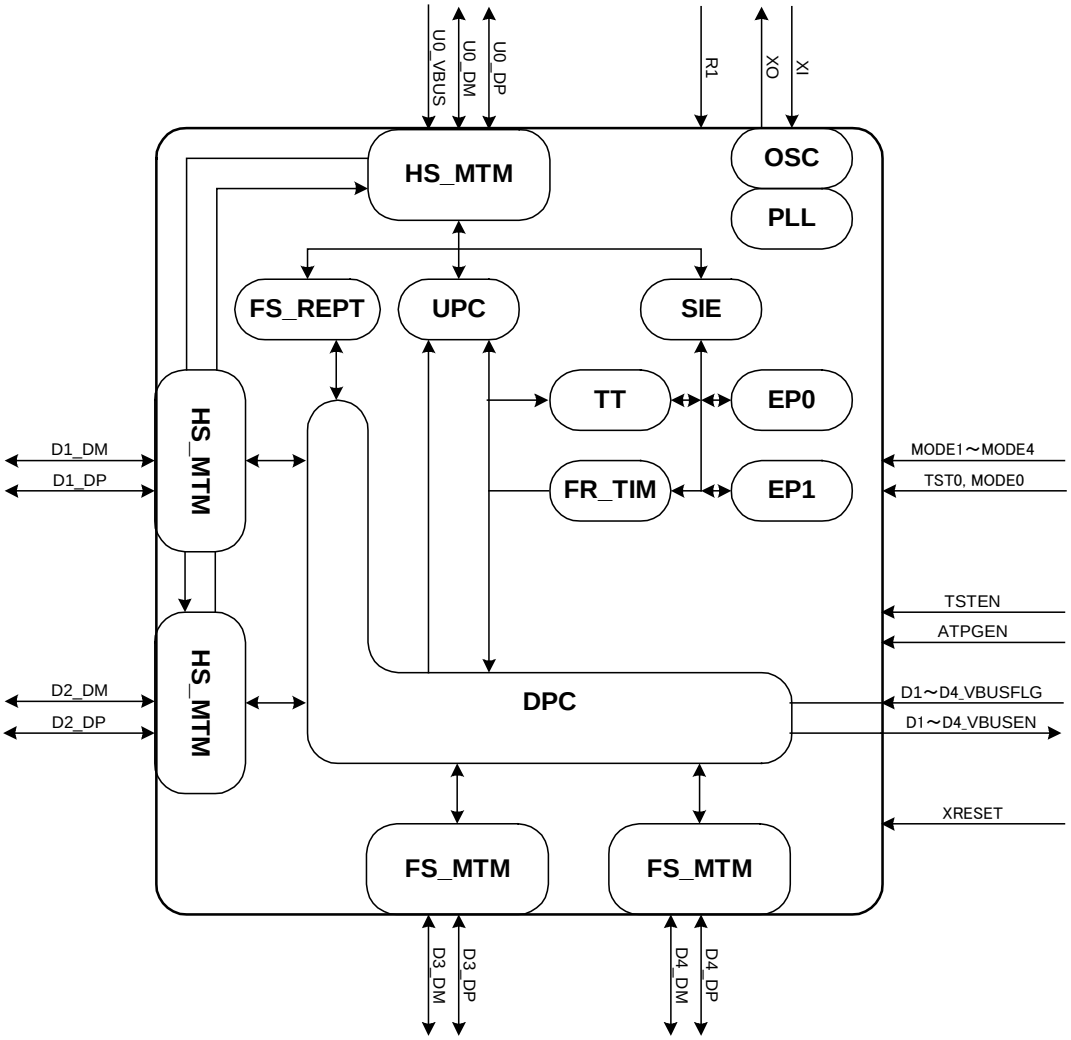


Figure 3.1 Block Diagram

DPC : Downstream port controller

EP0 : Endpoint 0 controller

EP1 : Endpoint 1 controller

FR_TIM : Frame timer

FS_REPT : FS/LS repeater circuit

FS_MTM : FS/LS transceiver macro circuit

HS_MTM : HS/FS/LS transceiver macro circuit

OSC : Oscillator circuit (with built-in feedback resistor)

PLL : Phase locked loop

SIE : Serial interface engine

TT : Transaction translator

UPC : Upstream port controller

4. Pin Layout Diagram

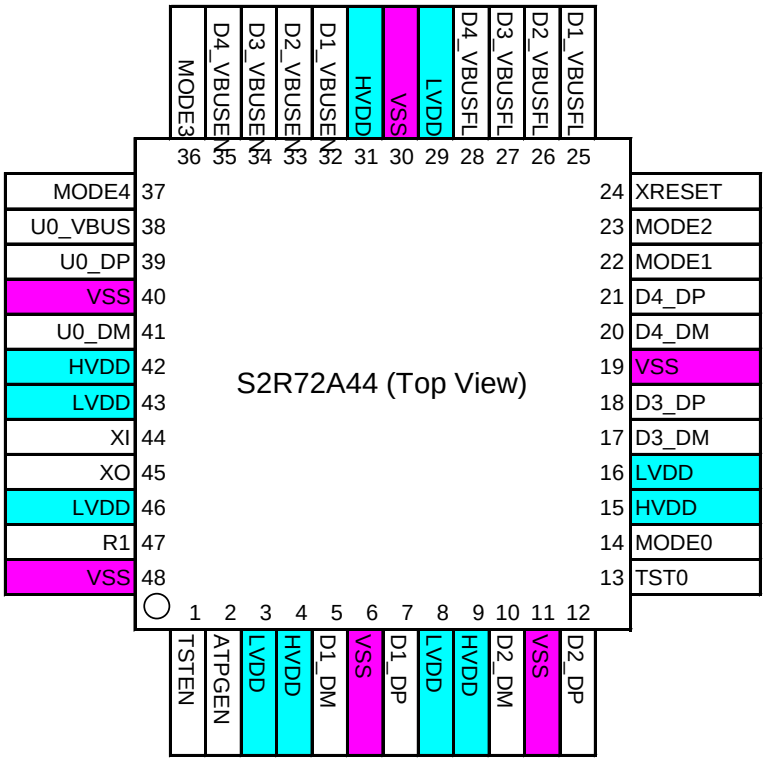


Figure 4.1 S2R72A44 package pin layout diagram (QFP12-48, SQFN7-48)

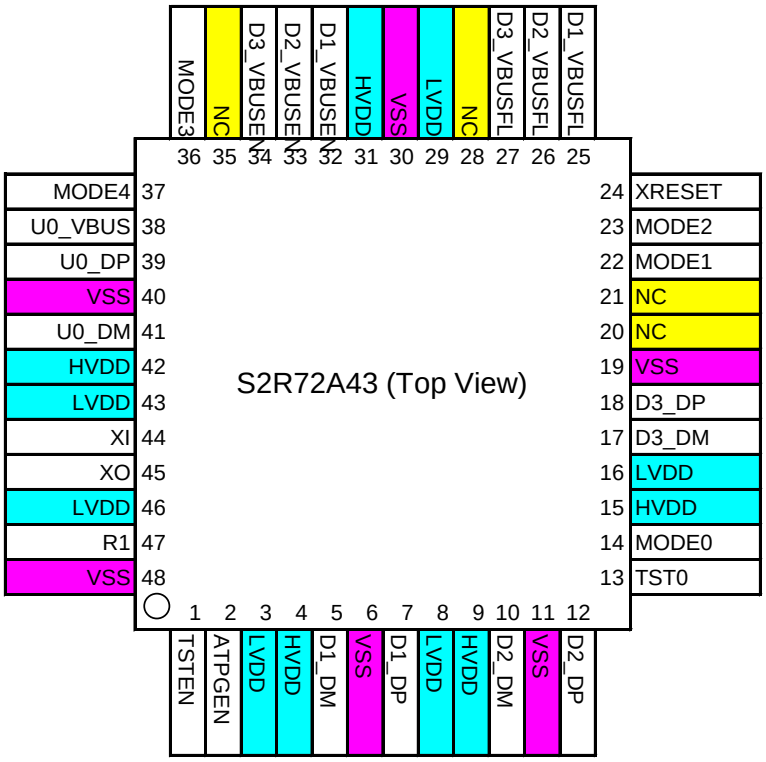


Figure 4.2 S2R72A43 package pin layout diagram (QFP12-48, SQFN7-48)

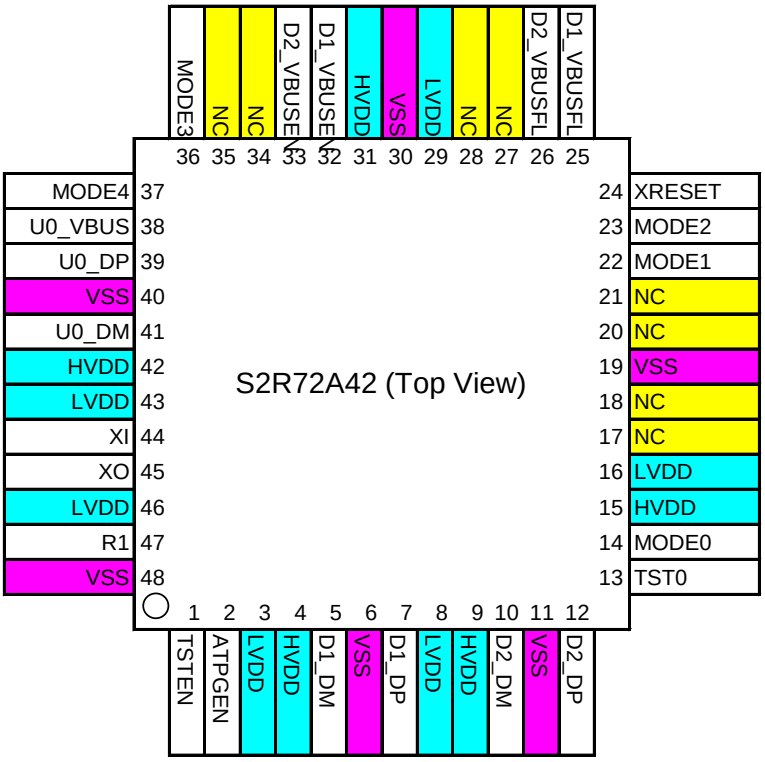


Figure 4.3 S2R72A42 package pin layout diagram (QFP12-48, SQFN7-48)

5. Pin Function and Description

GENERAL (applies to S2R72A44/A43/A42)

Pin No.	Name	I/O	RESET	Description
24	XRESET	IN	–	Reset signal

REFERENCE (applies to S2R72A44/A43/A42)

Pin No.	Name	I/O	RESET	Description
44	XI	IN	–	Internal oscillator circuit input (12 MHz)
45	XO	OUT	–	Internal oscillator circuit output (12 MHz)
47	R1	IN	–	Reference voltage setting pin (connect 12 kΩ±1% between VSS pins)

TEST (applies to S2R72A44/A43/A42)

Pin No.	Name	I/O	RESET	Description
1	TSTEN	IN (PD)	–	Test pin (*): Not used by user
2	ATPGEN	IN (PD)	–	Test pin (*): Not used by user
13	TST0	IN	–	Test pin (*): Not used by user

PD: Using pull-down I/O

*: Fix as Low or pull down on board.

MODE (applies to S2R72A44/A43/A42)

<table>
<tr><th>Pin No.</th><th>Name</th><th>I/O</th><th>RESET</th><th>Description</th></tr>
<tr><td>14</td><td>MODE0</td><td>IN</td><td>–</td><td>USB Revision setting (*3)
0: USB 2.0 (High-speed compatible hub) 1: USB 1.1 (Full-speed hub)</td></tr>
<tr><td>22</td><td>MODE1</td><td>IN</td><td>–</td><td rowspan="2">Down ports' VBUS setting pin
MODE1: bPwrOn2PwrGood selector setting pin
0: 0 ms, 1: 100 ms
MODE2: Gang/Individual selector pin
0: Gang, 1: Individual
<table><tr><th>MODE2</th><th>MODE1</th><th>VBUS Mode</th></tr><tr><td>H</td><td>H</td><td>Individual Mode</td></tr><tr><td>L</td><td>H</td><td>Gang Mode</td></tr><tr><td>H/L</td><td>L</td><td>Non-operation mode</td></tr></table></td></tr>
<tr><td>23</td><td>MODE2</td><td>IN</td><td>–</td></tr>
<tr><td rowspan="2">36</td><td rowspan="2">MODE3</td><td rowspan="2">IN</td><td rowspan="2">–</td><td rowspan="2">Port setting pin
<table><tr><th rowspan="2">MODE4</th><th rowspan="2">MODE3</th><th rowspan="2">Ports</th><th colspan="3">Setting availability</th></tr><tr><th>A44</th><th>A43</th><th>A42</th></tr><tr><td>0</td><td>0</td><td>2 ports</td><td>✓</td><td>✓</td><td>✓</td></tr><tr><td>0</td><td>1</td><td>3 ports</td><td>✓</td><td>✓</td><td>–</td></tr><tr><td>1</td><td>1</td><td>4 ports</td><td>✓</td><td>–</td><td>–</td></tr><tr><td>1</td><td>0</td><td>n/a</td><td>–</td><td>–</td><td>–</td></tr></table></td></tr>
<tr><td>37</td><td>MODE4</td><td>IN</td><td>–</td></tr>
</table>

*3: Operates at full-speed in USB 1.1 mode, even when connected to a USB 2.0 (high-speed) compatible USB host.

USB (applies to S2R72A44/A43/A42)

Pin No.	Name	I/O	RESET	Description
38	U0_VBUS	IN (PD)	–	Upstream port VBUS input pin
39	U0_DP	BI	Hi-Z	Upstream port USB data line Data +
41	U0_DM	BI	Hi-Z	Upstream port USB data line Data -
7	D1_DP	BI	Hi-Z	Downstream port 1 USB data line Data +
5	D1_DM	BI	Hi-Z	Downstream port 1 USB data line Data -
12	D2_DP	BI	Hi-Z	Downstream port 2 USB data line Data +
10	D2_DM	BI	Hi-Z	Downstream port 2 USB data line Data -
25	D1_VBUSFLG	IN (PU)	–	Downstream port 1 USB power switch fault detection input signal (CMOS Schmidt input) 1: Normal, 0: Error Connect USB power switch to this pin in Gang mode. Use when adding external USB power switch. Leave open if not used.
32	D1_VBUSEN	OUT	Low	Downstream port 1 USB power switch control output signal Connect USB power switch to this pin in Gang mode. Use when adding external USB power switch. Leave open if not used.
26	D2_VBUSFLG	IN (PU)	–	Downstream port 2 USB power switch fault detection input signal (CMOS Schmidt input) 1: Normal, 0: Error Use when adding external USB power switch. Leave open if not used.
33	D2_VBUSEN	OUT	Low	Downstream port 2 USB power switch control output signal Use when adding external USB power switch. Leave open if not used.

PD: Using pull-down I/O

PU: Using pull-up I/O

5. Pin Function and Description

USB (S2R72A44)

Pin No.	Name	I/O	RESET	Description
18	D3_DP	BI	Hi-Z	Downstream port 3 USB data line Data +
17	D3_DM	BI	Hi-Z	Downstream port 3 USB data line Data -
21	D4_DP	BI	Hi-Z	Downstream port 4 USB data line Data +
20	D4_DM	BI	Hi-Z	Downstream port 4 USB data line Data -
27	D3_VBUSFLG	IN (PU)	–	Downstream port 3 USB power switch fault detection input signal (CMOS Schmidt input) 1: Normal, 0: Error Use when adding external USB power switch. Leave open if not used.
34	D3_VBUSEN	OUT	Low	Downstream port 3 USB power switch control output signal Use when adding external USB power switch. Leave open if not used.
28	D4_VBUSFLG	IN (PU)	–	Downstream port 4 USB power switch fault detection input signal (CMOS Schmidt input) 1: Normal, 0: Error Use when adding external USB power switch. Leave open if not used.
35	D4_VBUSEN	OUT	Low	Downstream port 4 USB power switch control output signal Use when adding external USB power switch. Leave open if not used.

PU: Using pull-up I/O

USB (S2R72A43)

Pin No.	Name	I/O	RESET	Description
18	D3_DP	BI	Hi-Z	Downstream port 3 USB data line Data +
17	D3_DM	BI	Hi-Z	Downstream port 3 USB data line Data -
21	NC	–	–	Not used (leave open)
20	NC	–	–	Not used (leave open)
27	D3_VBUSFLG	IN (PU)	–	Downstream port 3 USB power switch fault detection input signal (CMOS Schmidt input) 1: Normal, 0: Error Use when adding external USB power switch. Leave open if not used.
34	D3_VBUSEN	OUT	Low	Downstream port 3 USB power switch control output signal Use when adding external USB power switch. Leave open if not used.
28	NC	–	–	Not used (leave open)
35	NC	–	–	Not used (leave open)

PU: Using pull-up I/O

USB (S2R72A42)				
Pin No.	**Name**	**I/O**	**RESET**	**Description**
18	NC	–	–	Not used (leave open)
17	NC	–	–	Not used (leave open)
21	NC	–	–	Not used (leave open)
20	NC	–	–	Not used (leave open)
27	NC	–	–	Not used (leave open)
34	NC	–	–	Not used (leave open)
28	NC	–	–	Not used (leave open)
35	NC	–	–	Not used (leave open)

POWER (applies to S2R72A44/A43/A42)			
Pin No.	**Name**	**Voltage**	**Description**
4, 9, 15, 31, 42	HVDD	3.3 V	3.3 V supply for USB and IO
3, 8, 16, 29, 43, 46	LVDD	1.8	1.8 V supply for internal core
6, 11, 19, 30, 40, 48	VSS	0 V	GND

Exposed Die Pad：SQFNx-PKG only

5.1 VBUS switch management

Dx{x=1-4}_VBUSEN pins corresponding to each down ports are surved for this purpose.

VBUS switch devices connected to those pins can be managed individually (Individual mode, i.e. MODE2 = High) or concurrently (Gang mode, i.e. MODE2 = Low).

Assertion of VBUSEN signals are caused only by SetPortFeature(PORT_POWER) standard request which is issued by the Host. Further conditions as listed below are required for VBUSEN signals to be asserted at that moment.

- MODE1 pin is set to High (i.e. bPwrOn2PwrGood = 0b1)
- The LSI is under configured condition (as USB standard meaning) as a result of receiving SetConfiguration() standard request from the Host.
- Dx{x=1-4}_VBUSFLG pins correspoinding to each of down ports are not forced to low.

If each of those VBUSFLG signals is asserted, PORT_OVER_CURRENT status on each down port is set. Those statuses can be checked with GetPortStatus() standard request which is issued repeatedly by ordinaly host stacks.

Lack of at least one of above conditions causes nagation of VBUSEN signal. Once VBUSEN is negated, it is not asserted again without reception of SetPortFeature(PORT_POWER) even if conditions are returned in order.

In Gang mode, D1_VBUSEN alone is served for the VBUS management function.

Please refer to the USB 2.0 standard for USB defined things such as bPwrOn2PwrGood condition, standard requests, Individual mode or Gang mode.

6. Descriptor

6.1 Device Descriptor

Field	Size	USB 2.0 mode		USB 1.1 mode	Remarks
	(Byte)	High-Speed	Full-Speed	Full-Speed	
bLength	1	12h	12h	12h	
bDescriptorType	1	01h	01h	01h	
bcdUSB	2	0200h	0200h	0110h	0200h: USB2.0 0110h: USB1.1
bDeviceClass	1	09h	09h	09h	
bDeviceSubClass	1	00h	00h	00h	
bDeviceProtocol	1	01h	00h	00h	
bMaxPackeSize0	1	40h	40h	40h	
idVendor	2	04B8h	04B8h	04B8h	EPSON
idProduct	2	090Ah	090Ah	090Ah	S2R72A0x / S2R72A4x series
bcdDevice	2	0090h	0090h	0090h	
iManufacturer	1	00h	00h	00h	
iProduct	1	00h	00h	00h	
iSerialNumber	1	00h	00h	00h	
bNumConfigurations	1	01h	01h	01h	

6.2 Device Qualifier Descriptor

Field	Size	USB 2.0 mode		USB 1.1 mode	Remarks
	(Byte)	High-Speed	Full-Speed	Full-Speed	
bLength	1	0Ah	0Ah	Not supported	
bDescritptor Type	1	06h	06h	Not supported	
bcdUSB	2	0200h	0200h	Not supported	0200h: USB2.0 0110h: USB1.1
bDeviceClass	1	09h	09h	Not supported	
bDeviceSubClass	1	00h	00h	Not supported	
bDeviceProtocol	1	00h	01h	Not supported	
bMaxPacketSize0	1	40h	40h	Not supported	
bNumConfigurations	1	01h	01h	Not supported	
bReserved	1	00h	00h	Not supported	

6.3 Configuration Descriptor

Field	Size	USB 2.0 mode		USB 1.1 mode	Remarks
	(Byte)	High-Speed	Full-Speed	Full-Speed	
Configuration Descriptor					
bLength	1	09h	09h	09h	
bDescriptorType	1	02h	02h	02h	
wTotalLength	2	0019h	0019h	0019h	
bNumInterface	1	01h	01h	01h	
bConfigurationValue	1	01h	01h	01h	
iConfiguration	1	00h	00h	00h	
bmAttribute	1	E0h	E0h	E0h	
bMaxPower	1	32h	32h	32h	
Interface Descriptor					
bLength	1	09h	09h	09h	
bDescriptorType	1	04h	04h	04h	
bInterfacdeNumber	1	00h	00h	00h	
bAlternateSetting	1	00h	00h	00h	
bNumEndpoints	1	01h	01h	01h	
bInterfaceClass	1	09h	09h	09h	
bInterfaceSubClass	1	00h	00h	00h	
bInterfaceProtocol	1	00h	00h	00h	
iInterface	1	00h	00h	00h	
Endpoint Descriptor					
bLength	1	07h	07h	07h	
bDescriptorType	1	05h	05h	05h	
bEndpointAddress	1	81h	81h	81h	
bmAttribute	1	03h	03h	03h	
wMaxPacketSize	2	0001h	0001h	0001h	
bInterval	1	0Ch	FFh	FFh	

6.4 Other Speed Configuration Descriptor

Field	Size	USB 2.0 mode		USB 1.1 mode	Remarks
	(Byte)	High-Speed	Full-Speed	Full-Speed	
Other_Speed_Configuration Descriptor					
bLength	1	09h	09h	Not supported	
bDescriptorType	1	07h	07h	Not supported	
wTotalLength	2	0019h	0019h	Not supported	
bNumInterface	1	01h	01h	Not supported	
bConfigurationValue	1	01h	01h	Not supported	
iConfiguration	1	00h	00h	Not supported	
bmAttribute	1	E0h	E0h	Not supported	
bMaxPower	1	32h	32h	Not supported	
Interface Descriptor					
bLength	1	09h	09h	Not supported	
bDescriptorType	1	04h	04h	Not supported	
bInterfaceNumber	1	00h	00h	Not supported	
bAlternateSetting	1	00h	00h	Not supported	
bNUMEndpoints	1	01h	01h	Not supported	
bInterfaceClass	1	09h	09h	Not supported	
bInterfaceSubClass	1	00h	00h	Not supported	
bInterfaceProtocol	1	00h	00h	Not supported	
iInterface	1	00h	00h	Not supported	
Endpoint Descriptor					
bLength	1	07h	07h	Not supported	
bDescriptorType	1	05h	05h	Not supported	
bEndpointAddress	1	81h	81h	Not supported	
bmAttribute	1	03h	03h	Not supported	
wMaxPacketSize	2	0001h	0001h	Not supported	
bInterval	1	FFh	0Ch	Not supported	

6.5 HUB Class Descriptor

Field	Size	USB 2.0 mode		USB 1.1 mode	Remarks
	(Byte)	High-Speed	Full-Speed	Full-Speed	
bDescLength	1	09h	09h	09h	
bDescriptorType	1	29h	29h	29h	
bNbrPorts	1	04h/03h/02h	04h/03h/02h	04h/03h/02h	Pin setting: {MODE4,MODE3}=11b/01b/00b
wHubCharacteristics	2	0029h/0020h	0029h/0020h	0009h/0000h	Pin setting: MODE2=High/Low
bPwrOn2PwrGood	1	32h/00h	32h/00h	32h/00h	Pin setting: MODE1=High/Low
bHubContrCurrent	1	64h	64h	64h	
DeviceRemovable	1	00h	00h	00h	
PortpwrCtrlMask	1	FFh	FFh	FFh	

7. Request List

The S2R72A44/A43/A42F12C4 LSI replies STALL for those unsupported requests which are shaded in the list.

7.1 Standard requests

Request	bmRequest Type	bRequest	wValue	wIndex	wLength
SET_DESCRIPTOR(DEVICE)	0x00	0x07	0x0100	0x0000	0x0012
SET_DESCRIPTOR(CONFIGRATION)	0x00	0x07	0x0200	0x0000	0x0019
SET_DESCRIPTOR(STRING_INDEX0)	0x00	0x07	0x0300	0x0409 or 0x0000	0x0004
SET_DESCRIPTOR(STRING_INDEX1)	0x00	0x07	0x0301	0x0409	(variable)
SET_DESCRIPTOR(STRING_INDEX2)	0x00	0x07	0x0302	0x0409	(variable)
SET_DESCRIPTOR(STRING_INDEX3)	0x00	0x07	0x0303	0x0409	(variable)
SET_DESCRIPTOR(STRING_INDEX4)	0x00	0x07	0x0304	0x0409	(variable)
SET_DESCRIPTOR(STRING_INDEX5)	0x00	0x07	0x0305	0x0409	(variable)
SET_DESCRIPTOR(INTERFACE)	0x00	0x07	0x0400	0x0000	0x0009
SET_DESCRIPTOR(ENDPOINT)	0x00	0x07	0x0500	0x0000	0x0007
SET_DESCRIPTOR(DEVICE_QUALIFIER)	0x00	0x07	0x0600	0x0000	0x000A
SET_DESCRIPTOR(OTHER_SPEED_ CONFIGRATION)	0x00	0x07	0x0700	0x0000	0x0019
SET_DESCRIPTOR(INTERFACE_POWER)	0x00	0x07	0x0800	0x0000	0x0019
GET_DESCRIPTOR(DEVICE)	0x80	0x06	0x0100	0x0000	0x0012
GET_DESCRIPTOR(CONFIGRATION)	0x80	0x06	0x0200	0x0000	0x0019
GET_DESCRIPTOR(STRING_INDEX0)	0x80	0x06	0x0300	0x0409 or 0x0000	0x0004
GET_DESCRIPTOR(STRING_INDEX1)	0x80	0x06	0x0301	0x0409	(variable)
GET_DESCRIPTOR(STRING_INDEX2)	0x80	0x06	0x0302	0x0409	(variable)
GET_DESCRIPTOR(STRING_INDEX3)	0x80	0x06	0x0303	0x0409	(variable)
GET_DESCRIPTOR(STRING_INDEX4)	0x80	0x06	0x0304	0x0409	(variable)
GET_DESCRIPTOR(STRING_INDEX5)	0x80	0x06	0x0305	0x0409	(variable)
GET_DESCRIPTOR(INTERFACE)	0x80	0x06	0x0400	0x0000	0x0009
GET_DESCRIPTOR(ENDPOINT)	0x80	0x06	0x0500	0x0000	0x0007
GET_DESCRIPTOR(DEVICE_QUALIFIER)	0x80	0x06	0x0600	0x0000	0x000A
GET_DESCRIPTOR(OTHER_SPEED_ CONFIGRATION)	0x80	0x06	0x0700	0x0000	0x0019
GET_DESCRIPTOR(INTERFACE_POWER)	0x80	0x06	0x0800	0x0000	0x0019
GET_STATUS(DEVICE)	0x80	0x00	0x0000	0x0000	0x0002
GET_STATUS(INTERFACE)	0x81	0x00	0x0000	0x0000	0x0002
GET_STATUS(ENDPOINT0)	0x82	0x00	0x0000	0x00n0 (n=0 or 8)	0x0002
GET_STATUS(ENDPOINT1)	0x82	0x00	0x0000	0x0000	0x0002
SYNCH FRAME	0x82	0x0C	0x0000	0x0000	0x0002
SET_ADDRESS()	0x00	0x05	0x00mn (m=0-7, n=0-F)	0x0000	0x0000
GET_CONFIGURATION ()	0x80	0x08	0x0000	0x0000	0x0001
SET_CONFIGURATION ()	0x00	0x09	0x000n (n=0 or 1)	0x0000	0x0000
GET_INTERFACE()	0x81	0x0A	0x0000	0x0000	0x0001
SET_INTERFACE()	0x01	0x0B	0x0000	0x0000	0x0000
SET_FEATURE(DEVICE_REMOTE_WAKEUP)	0x00	0x03	0x0001	0x0000	0x0000

CLEAR_FEATURE(DEVICE_REMOTE_WAKEUP)	0x00	0x01	0x0001	0x0000	0x0000
SET_FEATURE(ENDPOINT0 HALT)	0x02	0x03	0x0000	0x00n0 (n=0 or 8)	0x0000
CLEAR_FEATURE(ENDPOINT0 HALT)	0x02	0x01	0x0000	0x00n0 (n=0 or 8)	0x0000
SET_FEATURE(ENDPOINT1 HALT)	0x02	0x03	0x0000	0x0081	0x0000
CLEAR_FEATURE(ENDPOINT1 HALT)	0x02	0x01	0x0000	0x0081	0x0000
SET_FEATURE(TEST_J)	0x00	0x03	0x0002	0x0100	0x0000
SET_FEATURE(TEST_K)	0x00	0x03	0x0002	0x0200	0x0000
SET_FEATURE(TEST_SE0_NAK)	0x00	0x03	0x0002	0x0300	0x0000
SET_FEATURE(TEST_PACKET)	0x00	0x03	0x0002	0x0400	0x0000
SET_FEATURE(TEST_FORCE_ENABLE)	0x00	0x03	0x0002	0x0500	0x0000

7.2 Class-specific requests

Request	**bmRequest Type**	**bRequest**	**wValue**	**wIndex**	**wLength**
GetHubDescriptor()	0xA0	0x06	0x0000 or 0x2900	0x0000	0x0009
SetHubDescriptor()	0x20	0x07	0x0000 or 0x2900	0x0000	0xFFFF
GetHubStatus()	0xA0	0x00	0x0000	0x0000	0x0004
GetPortStatus(Port y)	0xA3	0x00	0x0000	0x000y	0x0004
GetBusStatus(Port y)	0xA3	0x02	0x0000	0x000y	0x0001
SetHubFeature(C_HUB_LOCAL_POWER)	0x20	0x03	0x0000	0x0000	0x0000
ClearHubFeature(C_HUB_LOCAL_POWER)	0x20	0x01	0x0000	0x0000	0x0000
SetHubFeature(C_HUB_OVER_CURRENT)	0x20	0x03	0x0001	0x0000	0x0000
ClearHubFeature(C_HUB_OVER_CURRENT)	0x20	0x01	0x0001	0x0000	0x0000
SetPortFeature(PORT_ CONNECTION)	0x23	0x03	0x0000	0x000y	0x0000
ClearPortFeature(PORT_ CONNECTION)	0x23	0x01	0x0000	0x000y	0x0000
SetPortFeature(PORT_ENABLE)	0x23	0x03	0x0001	0x000y	0x0000
ClearPortFeature(PORT_ENABLE)	0x23	0x01	0x0001	0x000y	0x0000
SetPortFeature(PORT_SUSPEND)	0x23	0x03	0x0002	0x000y	0x0000
ClearPortFeature(PORT_SUSPEND)	0x23	0x01	0x0002	0x000y	0x0000
SetPortFeature(PORT_RESET)	0x23	0x03	0x0004	0x000y	0x0000
ClearPortFeature(PORT_RESET)	0x23	0x01	0x0004	0x000y	0x0000
SetPortFeature(PORT_POWER)	0x23	0x03	0x0008	0x000y	0x0000
ClearPortFeature(PORT_POWER)	0x23	0x01	0x0008	0x000y	0x0000
SetPortFeature(PORT_LOW_SPEED)	0x23	0x03	0x0009	0x000y	0x0000
ClearPortFeature(PORT_ LOW_SPEED)	0x23	0x01	0x0009	0x000y	0x0000
SetPortFeature(PORT_HIGH_SPEED)	0x23	0x03	0x000A	0x000y	0x0000
ClearPortFeature(PORT_ HIGH_SPEED)	0x23	0x01	0x000A	0x000y	0x0000
SetPortFeature(C_PORT_CONNECTION)	0x23	0x03	0x0010	0x000y	0x0000
ClearPortFeature(C_PORT_CONNECTION)	0x23	0x01	0x0010	0x000y	0x0000
SetPortFeature(C_PORT_ENABLE)	0x23	0x03	0x0011	0x000y	0x0000
ClearPortFeature(C_PORT_ENABLE)	0x23	0x01	0x0011	0x000y	0x0000
SetPortFeature(C_PORT_SUSPEND)	0x23	0x03	0x0012	0x000y	0x0000
ClearPortFeature(C_PORT_SUSPEND)	0x23	0x01	0x0012	0x000y	0x0000
SetPortFeature(C_PORT_OVER_CURRENT)	0x23	0x03	0x0013	0x000y	0x0000
ClearPortFeature(C_PORT_OVER_CURRENT)	0x23	0x01	0x0013	0x000y	0x0000
SetPortFeature(C_PORT_RESET)	0x23	0x03	0x0014	0x000y	0x0000
ClearPortFeature(C_PORT_RESET)	0x23	0x01	0x0014	0x000y	0x0000
SetPortFeature(TEST_J)	0x23	0x03	0x0015	0x010y	0x0000

ClearPortFeature(TEST_J)	0x23	0x01	0x0015	0x010y	0x0000
SetPortFeature(TEST_K)	0x23	0x03	0x0015	0x020y	0x0000
ClearPortFeature(TEST_K)	0x23	0x01	0x0015	0x020y	0x0000
SetPortFeature(TEST_SE0_NAK)	0x23	0x03	0x0015	0x030y	0x0000
ClearPortFeature(TEST_SE0_NAK)	0x23	0x01	0x0015	0x030y	0x0000
SetPortFeature(TEST_PACKET)	0x23	0x03	0x0015	0x040y	0x0000
ClearPortFeature(TEST_PACKET)	0x23	0x01	0x0015	0x040y	0x0000
SetPortFeature(TEST_FORCE_ENABLE)	0x23	0x03	0x0015	0x050y	0x0000
ClearPortFeature(TEST_FORCE_ENABLE)	0x23	0x01	0x0015	0x050y	0x0000
SetPortFeature(PORT_INDICATOR)	0x23	0x03	0x0016	0x0*0y	0x0000
ClearPortFeature(PORT_INDICATOR)	0x23	0x01	0x0016	0x0*0y	0x0000
GetTTState()	0xA3	0x0A	0x0000	0x0001	0x08D0
ResetTT()	0x23	0x09	0x0000	0x0001	0x0000
ClearTTBuffer()	0x23	0x08	(EP No.)	0x0001	0x0000
StopTT()	0x23	0x0B	0x0000	0x0001	0x0000

*: “y” = 1-4(A44), 1-3(A43), 1-2(A42)

8. Electrical Characteristics

8.1 Absolute maximum ratings

Item	Code	Rating	Unit
Power supply voltage	HVDD	-0.3 to 4.0	V
	LVDD	-0.3 to 2.5	V
Input voltage	HVI	-0.3 to HVDD+0.5	V
	LVI *1	-0.3 to LVDD+0.5	V
	VVI *2	-0.3 to 6.0	V
Output voltage	HVO	-0.3 to HVDD+0.5	V
	LVO *3	-0.3 to LVDD+0.5	V
Output current/pin	Iout*4	±10	mA
Storage temperature	Tstg	-65 to 150	°C

*1: XI

*2: U0_VBUS

*3: XO

*4: Other than DP/DM pins on each port

8.2 Recommended operationg conditions

Item	Code	MIN	TYP	MAX	Unit
Power supply voltage	HVDD	3.00	3.30	3.60	V
	LVDD	1.65	1.80	1.95	V
Input voltage	HVI	-0.3	–	HVDD+0.3	V
	VVI *1	-0.3	–	5.25	V
	LVI *2	-0.3	–	LVDD+0.3	V
Ambient temperature	T_a	-40	25	105	°C

*1: U0_VBUS

*2: XI

[Power supply procedure precautions]

Refer to “Power on/off timing” in “AC characteristics.”

8.3 DC characteristics

8.3.1 Current consumption

Item			Code	Conditions	MIN	TYP	MAX	Unit
Power consumption *1								
	FS mode 2 valid down ports FS devices	HVDD	IHC02(F) *3	U0=FS D1/D2=FS D3/D4=none *C1	-	5	8	mA
		LVDD	ILC02(F)		-	22	34	mA
	FS mode 4 valid down ports FS devices	HVDD	IHC04(F) *3	U0=FS D1/D2=FS D3/D4=FS *C2	-	5	8	mA
		LVDD	ILC04(F)		-	22	34	mA
	HS mode 2 valid down ports HS devices	HVDD	IHC20(H)	U0=HS D1/D2=HS D3/D4=FS *C3	-	10	15	mA
		LVDD	ILC20(H)		-	40	60	mA
	HS mode 2 valid down ports FS devices	HVDD	IHC02(H) *3	U0=HS D1/D2=none D3/D4=FS *C4	-	5	8	mA
		LVDD	ILC02(H)		-	34	50	mA
	HS mode 4 valid down ports FS devices	HVDD	IHC22(H) *3	U0=HS D1/D2=HS D3/D4=FS *C5	-	14	22	mA
		LVDD	ILC22(H)		-	40	60	mA
Power supply current *2								
	Power supply current (HS) *1	HVDD	IDDH (H)	HS mode D1/D2=HS	–	60	90	mA
		LVDD	IDDL (H)		–	64	96	mA
	Power supply current (FS) *2	HVDD	IDDH (F)	FS mode D1/D2=FS	–	24	36	mA
		LVDD	IDDL (F)		–	40	60	mA
Power supply current (static current)								
	HVDD Power supply current		IDDSH	Power supply max conditions Fixed to power supply or GND	–	–	20	μA
	LVDD Power supply current		IDDSL	Power supply max conditions Fixed to power supply or GND	–	–	500	μA
Input leakage								
	Input leakage current		IL	Power supply max conditions	-5	–	5	μA

*C1 Copy files from D1 to D2. 86.2% bus domination on U0. 1.0MB/s transfer rate. (Figure 8-1(1))
*C2 Copy files from D1 to D2. 85.4% bus domination on U0. 1.0MB/s transfer rate. (Figure 8-1(2))
*C3 Copy files from D1 to D2. 25.5% bus domination on U0. 12.7MB/s transfer rate. (Figure 8-1(3))
*C4 Copy files from D4 to D3. 8.1% bus domination on U0. 1.0MB/s transfer rate. (Figure 8-1(4))
*C5 Copy files from D4 to D3. 6.38% bus domination on U0. 1.0MB/s transfer rate. (Figure 8-1(5))

*1: TYP values are mean current for actual operation at recommended operating conditions (Ta = 25°C). MAX values are estimated from TYP values. Those values are correlative to “bus domination” ratio because the S2R72A44/A43/A42F12C4 LSI saves power consumption in the idle state.

*2: TYP values are peak current for actual operation at recommended operating conditions (Ta = 25°C). MAX values are estimated from TYP values.

*3: Current consumption from HVDD power supply is influenced by cable length when transmittiong on FS mode.

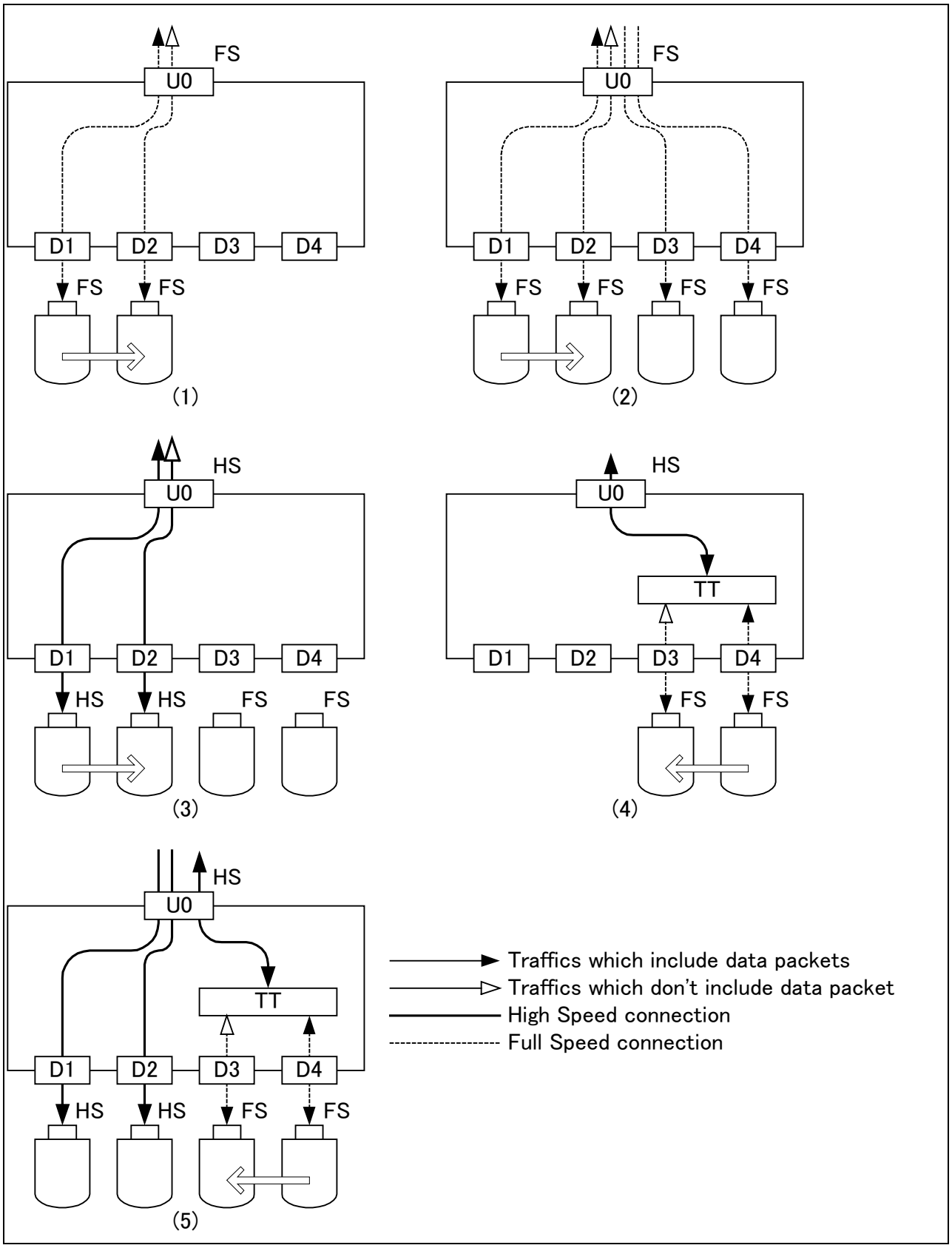

FS
U0
D1
D2
D3
D4
FS
FS
(1)
FS
U0
D1
D2
D3
D4
FS
FS
FS
FS
(2)
HS
U0
D1
D2
D3
D4
HS
HS
FS
FS
(3)
HS
U0
TT
D1
D2
D3
D4
FS
FS
(4)
HS
U0
TT
D1
D2
D3
D4
HS
HS
FS
FS
(5)
Traffics which include data packets
Traffics which don't include data packet
High Speed connection
Full Speed connection

Figure 8-1

8.3.2 Input characteristics

Item		Code	Conditions	MIN	TYP	MAX	Unit
Input characteristics (Schmidt)		Pins:	TSTEN, ATPGEN, TST0, MODE0, MODE1, MODE2, MODE3, MODE4, XRESET, D1_VBUSFLG, D2_VBUSFLG, D3_VBUSFLG, D4_VBUSFLG				
	"H" level trigger voltage	VT1+	HVDD = 3.6 V	–	–	2.52	V
	"L" level trigger voltage	VT1-	HVDD = 3.0 V	0.75	–	–	V
	Hysteresis voltage	ΔV1	HVDD = 3.0 V	0.30	–	–	V
Input characteristics (Schmidt USB FS)		Pins:	U0_DP, U0_DM, D1_DP, D1_DM, D2_DP, D2_DM, D3_DP, D3_DM, D4_DP, D4_DM,				
	"H" level trigger voltage	VT+ (USB)	HVDD = 3.6 V	–	–	2.00	V
	"L" level trigger voltage	VT- (UBS)	HVDD = 3.0 V	0.80	–	–	V
Clock input characteristics		Pin:	XI				
	"H" level trigger voltage	VT+(XI)	LVDD=1.95V	–	–	1.2	V
	"L" level trigger voltage	VT-(XI)	LVDD=1.65V	0.60	–	–	V
Input characteristics (USB: FS differential input)		Pins:	U0_DP/U0_DM pair D1_DP/D1_DM pair, D2_DP/D2_DM pair, D3_DP/D3_DM pair, D4_DP/D4_DM pair				
	Differential input sensitivity	VDSU	HVDD = 3.0 V Differential common mode range 0.8 V to 2.5 V	0.20	–	–	V
Input characteristics (Schmidt)		Pins:	U0_VBUS				
	"H" level trigger voltage	VT+ (VBUS)	HVDD = 3.6 V	-	–	2.88	V
	"L" level trigger voltage	VT- (VBUS)	HVDD = 3.0 V	1.37	–	-	V
Input characteristics		Pins:	D1_VBUSFLG, D2_VBUSFLG, D3_VBUSFLG, D4_VBUSFLG				
	Pull-up resistance	RPLU	VI = VSS	32	80	192	kΩ
Input characteristics		Pins:	U0_DP				
	Pull-up resistance	RPLUU	VI = VSS	1.425	-	1.575	kΩ
Input characteristics		Pins:	D1_DP, D1_DM, D2_DP, D2_DM, D3_DP, D3_DM, D4_DP, D4_DM				
	Pull-down resistance	RPLDD	VI = HVDD	14.25	-	15.75	kΩ
Input characteristics		Pins:	TSTEN, ATPGEN				
	Pull-down resistance	RPLDU	VI = HVDD	32	80	192	kΩ
Input characteristics		Pins:	U0_VBUS				
	Pull-down resistance	RPLD	VVI = 5.0 V	100	-	165	kΩ

8.3.3 Output characteristics

(V_{SS}=0V)

Item		Code	Conditions	MIN	TYP	MAX	Unit
Output characteristics		Pins:	D1_VBUSEN, D2_VBUSEN, D3_VBUSEN, D4_VBUSEN				
	"H" level output voltage	VOH1	HVDD = 3.0 V IOH = -1.4mA	HVDD -0.4	–	–	V
	"L" level output voltage	VOL1	HVDD = 3.0 V IOL = 1.4 mA	-	–	0.4	V
Output characteristics (USB: HS)		Pins:	U0_DP, D0_DM, D1_DP, D1_DM, D2_DP, D2_DM				
	HS output current (GND basis)	IOUH	HVDD = 3.3 V	-20	–	-18	mA
	HS termination resistance (GND basis)	ROUH	HVDD = 3.3 V	40.5	–	49.5	ohm
Output characteristics (USB: FS)		Pins:	U0_DP, D0_DM, D1_DP, D1_DM, D2_DP, D2_DM, D3_DP, D3_DM, D4_DP, D4_DM				
	"H" level output resistance	ROHUF	HVDD = 3.3 V	40.5	–	49.5	ohm
	"L" level output resistance	ROLUF	HVDD = 3.3 V	40.5	–	49.5	ohm
Output characteristics (USB LS)		Pins:	U0_DP, D0_DM, D1_DP, D1_DM, D2_DP, D2_DM, D3_DP, D3_DM, D4_DP, D4_DM				
	"H" level output resistance	ROHUL	HVDD=3.3V	60.0	-	100.0	ohm
	"L" level output resistance	ROLUL	HVDD=3.3V	60.0	-	100.0	ohm
Output characteristics		Pins:	XO				
	"H" level output current	IOH1	LVDD=1.8V VIH=LVDD-0.4V	-1.70	-	-1.20	mA
	"L" level output current	IOL1	LVDD=1.8V VIH=0.4V	1.25	-	1.75	mA
Output characteristics		Pins:	D1_VBUSEN, D2_VBUSEN, D3_VBUSEN, D4_VBUSEN				
	Off-state leakage current	IOZ	HVDD = 3.6 V VOH = HVDD VOL = VSS	-10	–	10	uA

8.3.4 Pin capacitance

Item		Code	Conditions	MIN	TYP	MAX	Unit
Pin capacitance		Pin names:	Input pins except USB				
	Input pin capacitance	CI	f = 1 MHz	–	–	8	pF
Pin capacitance		Pin names:	Output pins				
	Output pin capacitance	CO	f = 1 MHz	–	–	8	pF
Pin capacitance		Pin names:	Input/output pins except USB				
	Input/output pin capacitance	CB	f = 1 MHz	–	–	8	pF
Pin capacitance		Pin names:	U0_DP, U0_DM, D1_DP, D1_DM, D2_DP, D2_DM				
	Input/output pin capacitance (USB)	CBUH	f = 1 MHz	–	–	12	pF
Pin capacitance			D3_DP, D3_DM, D4_DP, D4_DM				
	Input/output pin capacitance (USB)	CBUF	f = 1 MHz	–	–	15	pF

8.4 AC characteristics

8.4.1 Power on/off timing

A. **Power on/off timing (recommended sequence: LVDD → HVDD/HVDD → LVDD)**

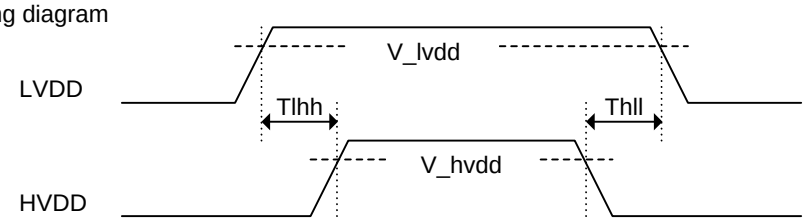
Timing parameters

Item	Code	min	typ	max	Unit
HVDD power on timing	Tlhh	0	–	10	sec
HVDD power off timing	Thll	0	–	10	sec

Voltage parameters

Item	Code	Voltage conditions		Unit
		On	Off	
LVDD initial voltage	V_lvdd	LVDD_min	LVDD_min	V
HVDD initial voltage	V_hvdd	HVDD_min	HVDD_min	V

Timing diagram



B. **Power on/off timing (HVDD → LVDD/LVDD → HVDD)**

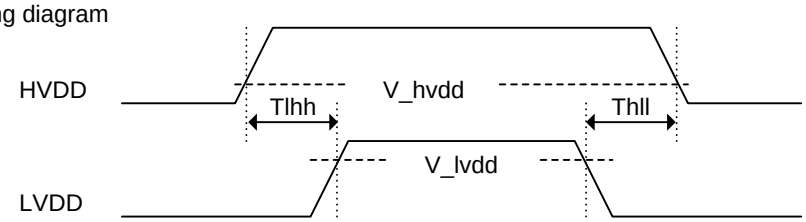
Timing parameters

Item	Code	min	typ	max	Unit
LVDD power on timing	Tlhh	0	–	1	sec
LVDD power off timing	Thll	0	–	1	sec

Voltage parameters

Item	Code	Voltage conditions		Unit
		On	Off	
LVDD initial voltage	V_lvdd	LVDD_min	LVDD_min	V
HVDD initial voltage	V_hvdd	0.3	0.3	V

Timing diagram

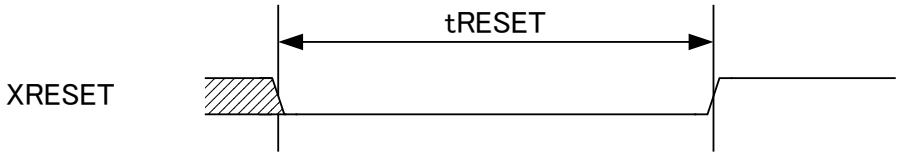


* When both timings for power on and off are LVDD → HVDD, refer to A for power on and B for power off. Likewise, when both timings for power on and off are HVDD → LVDD, refer to B for power on and A for power off.

* LVDD_min is the minimum value for LVDD, and HVDD_min is the minimum value for HVDD, which are defined respectively in 7.2.

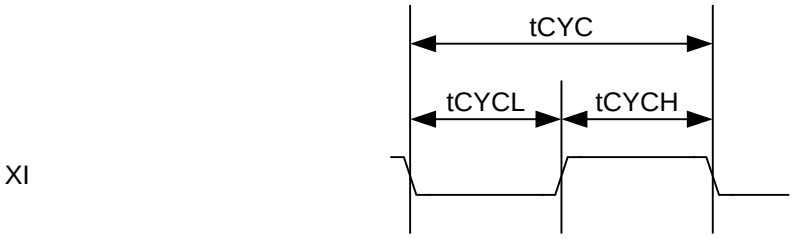
* Recommended sequence of power on/off timing is above A. In case of above B, the Tlhh and Thll are longer than 1 sec, it will be affect long term reliability.Only when both power supplies (HVDD and LVDD) are turned on, the operation and function include status of internal register and external I/O can gurantee.

8.4.2 Reset timing



Code	Description	min	typ	max	Unit
tRESET	Reset pulse width	400	–	–	ns

8.4.3 Clock timing

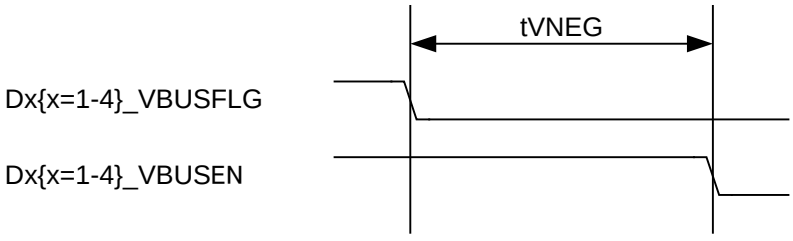


Code	Description	min	typ	max	Units
tCYC	Clock cycle	-	12.000	-	MHz
tCYCL tCYCH	Clock duty	-	50	-	%

8.4.4 USB I/F timing

Complies with USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard.

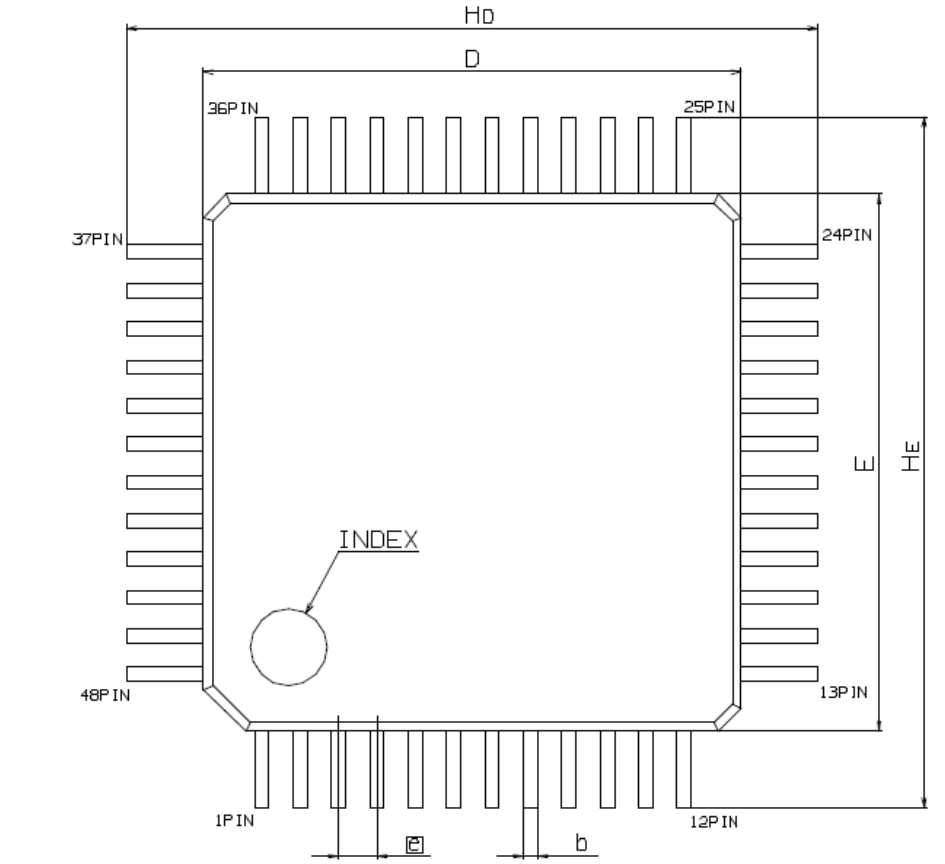
8.4.5 Over current detection timing

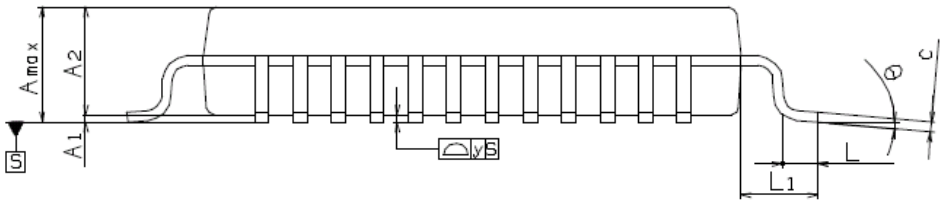


Code	Description	min	typ	max	Units
tVNEG	VBUSFLG assertion to VBUSEN negation	4	-	6	ms

9. External Dimensions Diagram

9.1 QFP12-48

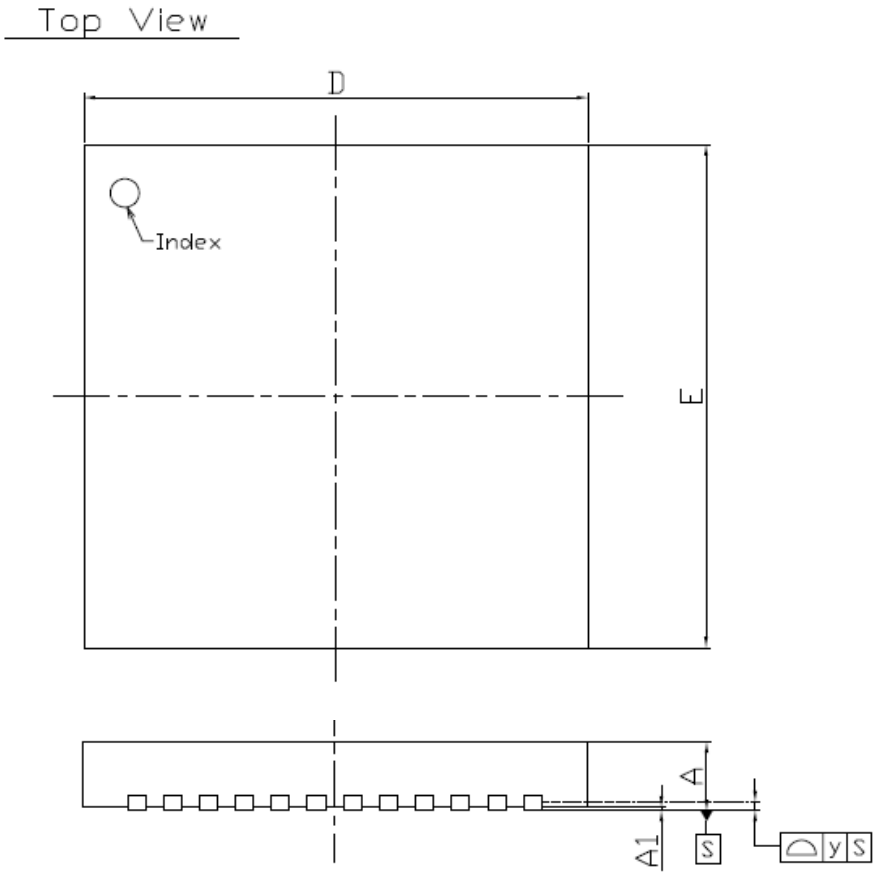


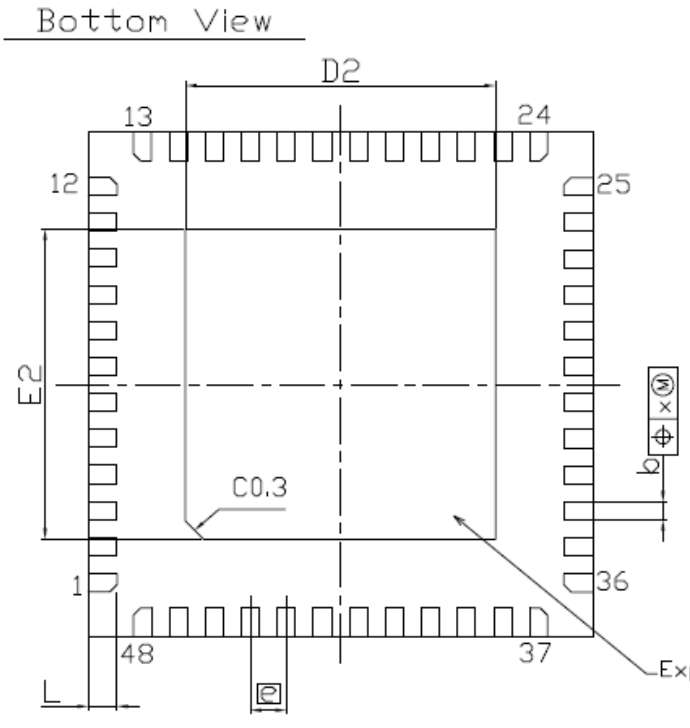


Symbol	Dimension in Millimters		
	Min	Nom	Max
E	-	7	-
D	-	7	-
A_{max}	-	-	1.7
A_1	-	0.1	-
A_2	-	1.4	-
e	-	0.5	-
b	0.13	-	0.27
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.7
L_1	-	1	-
H_E	-	9	-
H_D	-	9	-
y	-	-	0.08

1 = 1mm

9.2 SQFN7-48





Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.90	7.00	7.10
E	6.90	7.00	7.10
A	–	–	1.00
A_1	0.00	–	–
b	0.20	0.25	0.30
e	–	0.50	–
L	0.35	0.40	0.45
D2	4.20	4.30	4.40
E2	4.20	4.30	4.40
x	–	–	0.10
y	–	–	0.08

Exposed Die Pad is soldered to the mounting board
Exposed Die Pad has to connect to VSS on system of customer.

Exposed Die Pad is not soldered to the mounting board
The signal wirings and the other pattern do not have to be drawn under the Exposed Die Pad.

1 = 1mm

Revision History

Attachment-1

Rev. No.	Date	Page	Type	Revision details (including previous details) and reason
Rev. 0.01	03/31/2009	All	New	New issue
Rev. 0.79	06/17/2009	All	Correction	Corrected error in pin description for MODE4, 3 pins. Added USB 1.1 mode function. Added section “6. Descriptor,” and renumbered subsequent sections. Added some TBD items.
Rev. 0.90	09/11/2009	All	Correction	Fixed correction items in revision 0.79, and deleted descriptions kept as revision history with strike through. Added explanatory note for 7.4.1.
Rev.0.97	08/31/2010	All	Correction	Inserted chapter 7 “Request list”. Added some supplemental descriptions. Added some TBD items. Updated Series name.
Rev.1.00	03/31/2011	All	Release	Officially released
		p.12	Correction	Corrected lacked value on wHubCharacteristics on 6.5.
		p.13 p.18	Correction	Corrected typo on seriease name. S2R72A44/A43/A42F12E3 > S2R72A44/A43/A42F12C4
		p.16	Correction	Corrected typo on chapter title on 8. “Pin Function and Description” > “Electrical Characteristics”
		p.17	Definition	Defined T.B.D items on 8.3.1.
		p.20	Correction	Corrected conditions on VT+(XI) and VT-(XI).
		p.20	Correction	Corrected VT+(VBUS) and VT-(VBUS) definition.
		p.20	Correction	Corrected conditions on VDSU on 8.3.2
		p.20	Definition	Defined T.B.D items on 8.3.2
		p.20	Addition	Added RPLUU and RPLDD definition
		p.20	Undefinition	Undefined typ value on RPLD.
		p.21 p.22	Correction	Corrected typo on section number on 8.3.3 and 8.3.4.
		p.21	Redefinition	Replaced output characteristics ROHUH and ROLUH with IOUH and ROUH.
		p.24	Correction	Corrected error in AC spec. definition on 8.4.2.
Rev.1.10	02/06/2012	p.6	Correction	Corrected footnotes for pin.1 TSTEN and pin.2 ATPGEN as: “Fix as Low or pull down on board” from “Pulled down within LSI, but should preferably be fixed as Low on board”
Rev.1.20	05/27/2013	P1	Addition	Added S2R72A44F07E2, S2R72A43F07E2 and S2R72A42F07E2
		P2	Addition	Added SQFN package
		P4	Addition	Added SQFN7-48 (Figure.4.1 and Figure.4.2)

		P5	Addition	Added SQFN7-48 (Figure.4.3)
		P26	Addition	Added 9.2 SQFN7-48
Rev.1.30	07/11/2014	P23	Addition	Added note about sequence of power on/off timing
Rev.1.40	09/20/2017	P9	Addtion	Added Eposed Die Pad
		P26	Correction	SQFN-PKG Fig

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