

# **S2R72A54**

## **Data Sheet**

**S2R72A54F12E3xx**

**S2R72A54F06E3xx**

**S2R72A54F96E3xx**

## NOTICE

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# Table of Contents

<b>1. Overview</b> .....	<b>1</b>
<b>2. Features</b> .....	<b>2</b>
<b>3. Block Diagram</b> .....	<b>3</b>
<b>4. Pin Layout Diagram</b> .....	<b>4</b>
4.1 QFP12-48 Pin Layout Diagram .....	4
4.2 SQFN6-36/SQFN6-36-W Pin Layout Diagram .....	5
<b>5. Pin Function and Description</b> .....	<b>6</b>
5.1 VBUS switch management .....	8
<b>6. Descriptor</b> .....	<b>9</b>
6.1 Device Descriptor .....	9
6.2 Device Qualifier Descriptor .....	9
6.3 Configuration Descriptor .....	10
6.4 Other Speed Configuration Descriptor .....	11
6.5 HUB Class Descriptor .....	11
<b>7. Request List</b> .....	<b>12</b>
7.1 Standard requests .....	12
7.2 Class-specific requests .....	13
<b>8. Electrical Characteristics</b> .....	<b>15</b>
8.1 Absolute maximum ratings .....	15
8.2 Recommended operating conditions .....	15
8.3 DC characteristics .....	16
8.3.1 Power consumption .....	16
8.3.2 Input characteristics .....	17
8.3.3 Output characteristics .....	18
8.3.4 Pin capacitance .....	18
8.4 AC characteristics .....	19
8.4.1 Reset timing .....	19
8.4.2 Clock timing .....	19
8.4.3 USB I/F timing .....	19
8.4.4 Over current detection timing .....	19
<b>9. External Dimensions Diagram</b> .....	<b>20</b>
9.1 QFP12-48 external dimensions diagram .....	20
9.2 SQFN6-36 external dimensions diagram .....	21
9.3 SQFN6-36-W external dimensions diagram .....	22
<b>Revision History</b> .....	<b>23</b>

### 1. Overview

The S2R72A54 is USB hub controller LSIs supporting USB 2.0 (Universal Serial Bus Specification Revision 2.0) high-speed mode. They meet the stringent quality requirements for automotive use and are capable of operating at temperatures up to 105°C.

The S2R72A54 features both 1 upstream port and 4 downstream ports supporting high-speed mode.

Using the S2R72A54 enables USB host port of the main chip to be easily expanded to allow the connection of multiple USB devices such as mobile phone, audio players, or ETC devices to car navigation systems.

## 2. Features

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### 2. Features

- **AEC-Q100 certified**
- **Excellent data communication characteristics**
- **Wide temperature range**  
**Operating temperature range is -40°C to +105°C**
- **USB specifications**  
**Upstream port**  
Supports HS (480 Mbps) and FS (12 Mbps), and automatic detection  
Built-in termination (no external resistor required)  
**Downstream ports**  
Support HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps), all 4 ports  
Built-in termination (no external resistor required), all 4 ports  
**Built-in single transaction translator with four non-periodic buffers**  
**Supports Gang or Individual as overcurrent control**
- **Other specifications**  
**Supports 24 MHz crystal oscillator (with built-in oscillator circuit and feedback resistor)**  
**Power supply voltage: 3.3 V (3.0V to 3.6V)**  
**Built-in regulator to generate internal core voltage 1.8 V and PLL/OSC voltage 1.8 V.**  
**Package:**

<b>QFP12-48</b>	<b>(48-pin, 7 mm square, 0.5 mm pitch, 1.4 mm thickness)</b> <b>Product number: S2R72A54F12E3xx</b>
<b>SQFN6-36</b>	<b>(36-pin, 6 mm square, 0.5 mm pitch, 1.0 mm thickness)</b> <b>Product number: S2R72A54F06E3xx</b>
<b>SQFN6-36-W</b>	<b>(Wettable Flank, 36-pin, 6 mm square, 0.5 mm pitch, 1.0 mm thickness)</b> <b>Product number: S2R72A54F96E3xx</b>

\* The “xx” of two digits of end of the product number is different depending on the packing specification.

3. Block Diagram

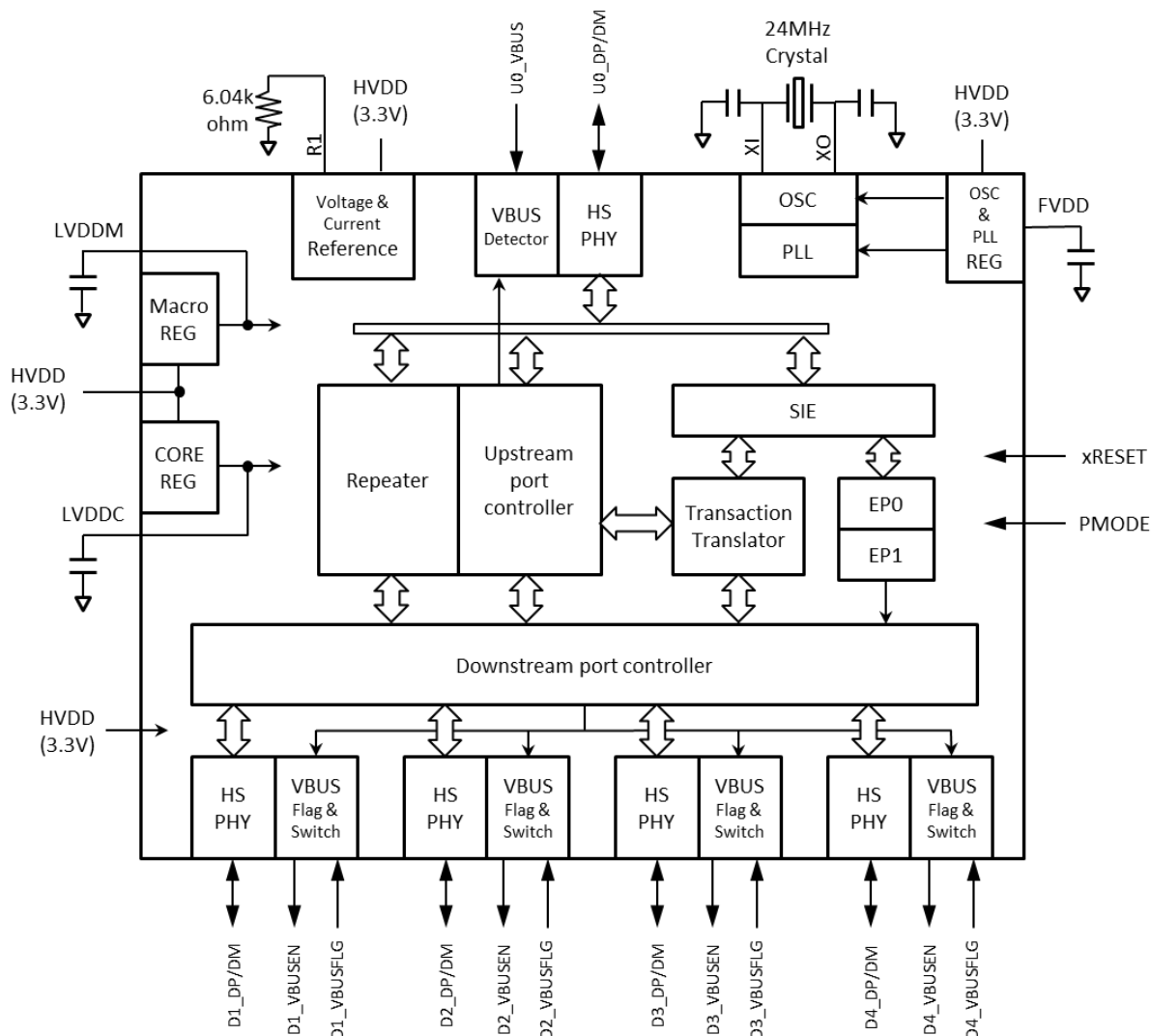


Figure 3.1 Block Diagram

- EP0 : Endpoint 0 controller
- EP1 : Endpoint 1 controller
- OSC : Oscillator circuit (with built-in feedback resistor)
- PLL : Phase locked loop
- SIE : Serial interface engine

## 4. Pin Layout Diagram

### 4. Pin Layout Diagram

#### 4.1 QFP12-48 Pin Layout Diagram

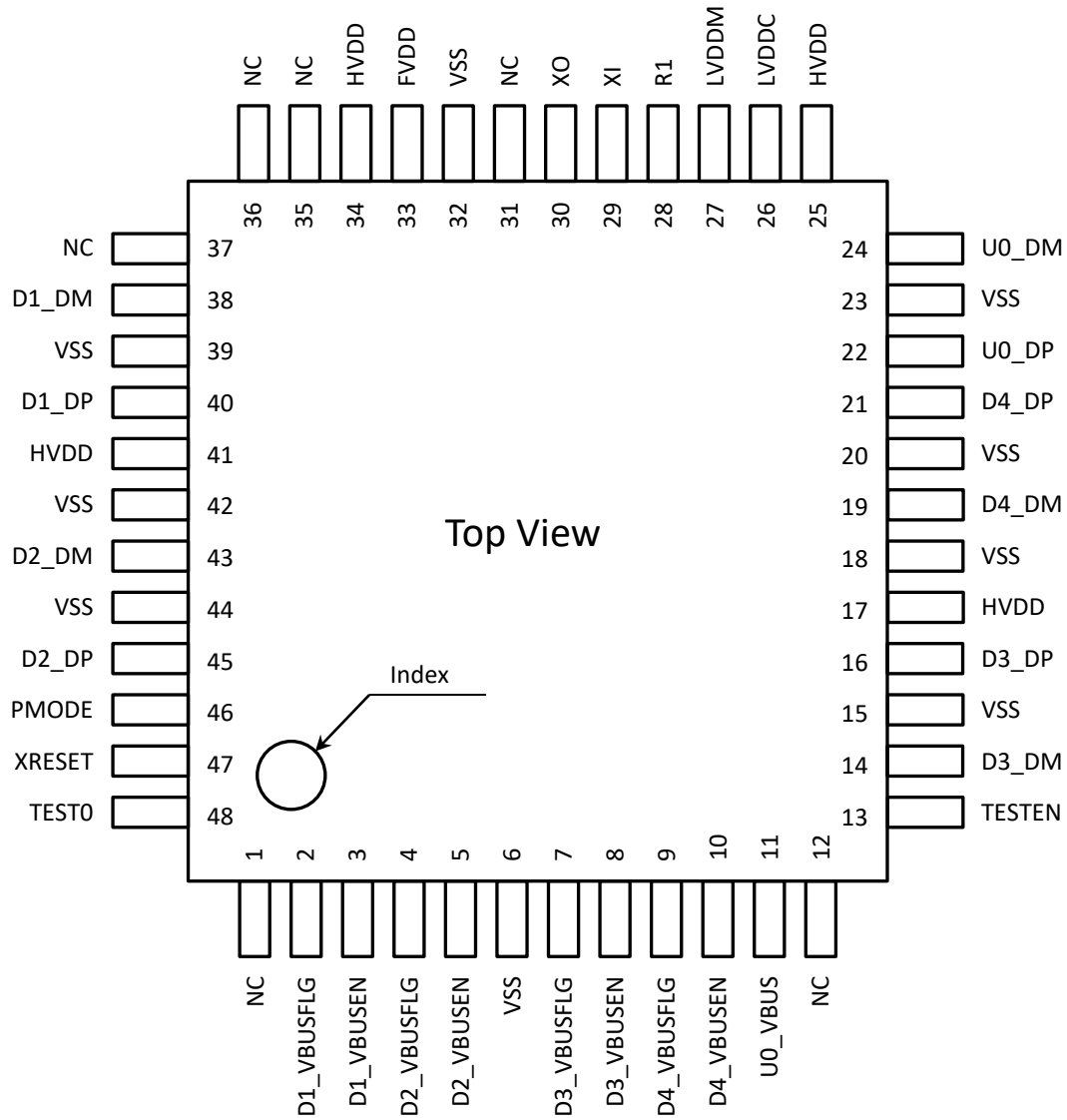


Figure 4.1 QFP12-48 pin layout diagram

4.2 SQFN6-36/SQFN6-36-W Pin Layout Diagram

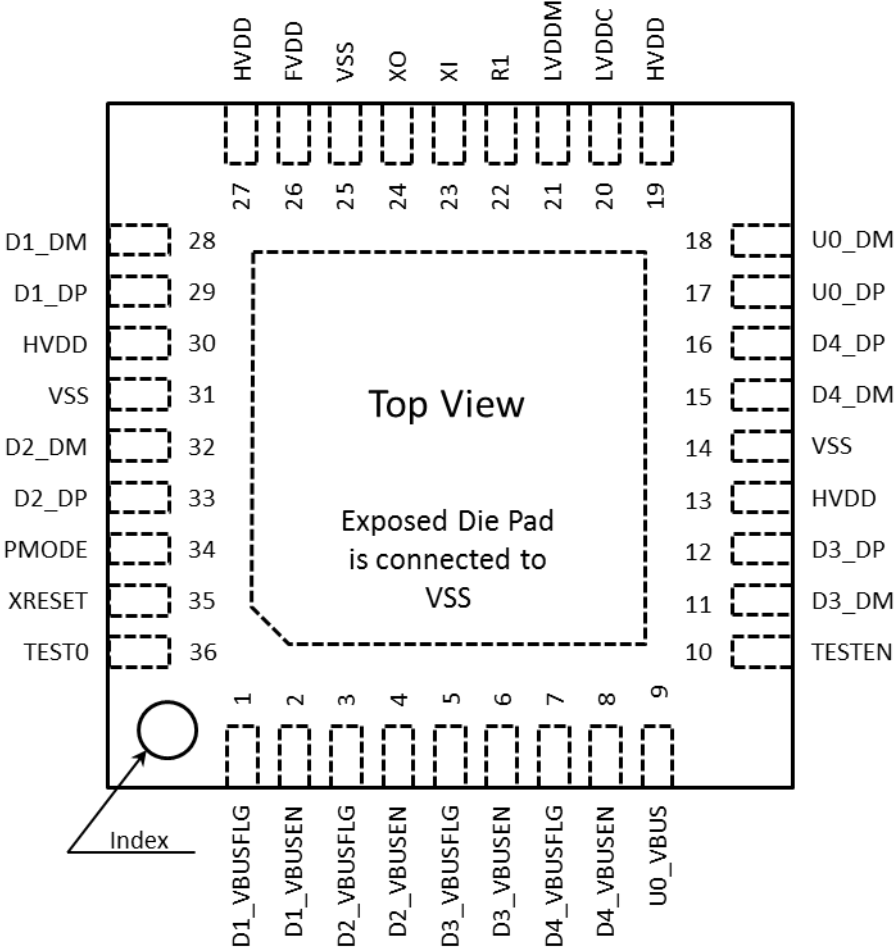


Figure 4.2 SQFN6-36/SQFN6-36-W pin layout diagram



## 5. Pin Function and Description

### 5. Pin Function and Description

GENERAL					
QFP	SQFN	Name	I/O	RESET	Description
47	35	XRESET	IN	–	Reset signal

REFERENCE					
QFP	SQFN	Name	I/O	RESET	Description
29	23	XI	IN	–	Internal oscillator circuit input (24 MHz)
30	24	XO	OUT	–	Internal oscillator circuit output (24 MHz)
28	22	R1	IN	–	Reference voltage setting pin Connect 6.04 kΩ±1% resistor between VSS

TEST					
QFP	SQFN	Name	I/O	RESET	Description
13	10	TESTEN	IN(PD)	–	Test pin (*): Not used by user
48	36	TEST0	IN	–	Test pin (*): Not used by user

PD: Using pull-down I/O

\*: Fix as Low or pull down on board.

MODE					
QFP	SQFN	Name	I/O	RESET	Description
46	34	PMODE	IN	–	Gang/Individual selector pin 0 : Gang 1 : Individual

USB					
QFP	SQFN	Name	I/O	RESET	Description
22	17	U0_DP	BI	Hi-Z	Upstream port USB data line Data +
24	18	U0_DM	BI	Hi-Z	Upstream port USB data line Data -
40	29	D1_DP	BI	Hi-Z	Downstream port 1 USB data line Data +
38	28	D1_DM	BI	Hi-Z	Downstream port 1 USB data line Data -
45	33	D2_DP	BI	Hi-Z	Downstream port 2 USB data line Data +
43	32	D2_DM	BI	Hi-Z	Downstream port 2 USB data line Data -
16	12	D3_DP	BI	Hi-Z	Downstream port 3 USB data line Data +
14	11	D3_DM	BI	Hi-Z	Downstream port 3 USB data line Data -
21	16	D4_DP	BI	Hi-Z	Downstream port 4 USB data line Data +
19	15	D4_DM	BI	Hi-Z	Downstream port 4 USB data line Data -

## 5. Pin Function and Description

USB (continued)					
QFP	SQFN	Name	I/O	RESET	Description
11	9	U0_VBUS	IN	–	Upstream port VBUS input pin Divide voltage externally in connecting VBUS of usb host. Connect HVDD if not used.
2	1	D1_VBUSFLG	IN(PU)	–	Downstream port 1 USB power switch fault detection input signal (CMOS Schmitt input) 1: Normal, 0: Error Connect USB power switch to this pin in Gang mode. Use when adding external USB power switch. Leave open if not used.
3	2	D1_VBUSEN	OUT	Low	Downstream port 1 USB power switch control output signal Connect USB power switch to this pin in Gang mode. Use when adding external USB power switch. Leave open if not used.
4	3	D2_VBUSFLG	IN(PU)	–	Downstream port 2 USB power switch fault detection input signal (CMOS Schmitt input) 1: Normal, 0: Error Use when adding external USB power switch. Leave open if not used.
5	4	D2_VBUSEN	OUT	Low	Downstream port 2 USB power switch control output signal Use when adding external USB power switch. Leave open if not used.
7	5	D3_VBUSFLG	IN(PU)	–	Downstream port 3 USB power switch fault detection input signal (CMOS Schmitt input) 1: Normal, 0: Error Use when adding external USB power switch. Leave open if not used.
8	6	D3_VBUSEN	OUT	Low	Downstream port 3 USB power switch control output signal Use when adding external USB power switch. Leave open if not used.
9	7	D4_VBUSFLG	IN(PU)	–	Downstream port 4 USB power switch fault detection input signal (CMOS Schmitt input) 1: Normal, 0: Error Use when adding external USB power switch. Leave open if not used.
10	8	D4_VBUSEN	OUT	Low	Downstream port 4 USB power switch control output signal Use when adding external USB power switch. Leave open if not used.

PD: Using pull-down I/O

PU: Using pull-up I/O

NC					
QFP	SQFN	Name	I/O	RESET	Description
1 12 31 35 36 37	–	NC	–	–	Not used (leave open)

## 5. Pin Function and Description

POWER				
QFP	SQFN	Name	Voltage	Description
17 25 34 41	13 19 27 30	HVDD	3.3V	3.3 V supply
33	26	FVDD	2.25V	Intermediate power of 1.8V generated for PLL and OSC Connect 10uF and 0.1uF capacitor between VSS.
26	20	LVDDC	1.85V	1.8V generated for logic core. Connect 10uF and 0.1uF capacitor between VSS.
27	21	LVDDM	1.85V	1.8V generated for USB phy. Connect 10uF and 0.1uF capacitor between VSS.
6 15 18 20 23 32 39 42 44	14 25 31 EP	VSS	0V	GND

EP: Exposed Pad

### 5.1 VBUS switch management

$Dx\{x=1-4\}$ \_VBUSEN pins corresponding to each down ports are served for this purpose.

VBUS switch devices connected to those pins can be managed individually (Individual mode, i.e. PMODE = High) or concurrently (Gang mode, i.e. PMODE = Low).

Assertion of VBUSEN signals are caused only by SetPortFeature(PORT\_POWER) standard request which is issued by the Host. Further conditions as listed below are required for VBUSEN signals to be asserted at that moment.

- The LSI is under configured condition (as USB standard meaning) as a result of receiving SetConfiguration() standard request from the Host.
- $Dx\{x=1-4\}$ \_VBUSFLG pins corresponding to each of down ports are not forced to low.

If each of those VBUSFLG signals is asserted, PORT\_OVER\_CURRENT status on each down port is set. Those statuses can be checked with GetPortStatus() standard request which is issued repeatedly by ordinaly host stacks.

Lack of at least one of above conditions causes negation of VBUSEN signal. Once VBUSEN is negated, it is not asserted again without reception of SetPortFeature(PORT\_POWER) even if conditions are returned in order.

In Gang mode, D1\_VBUSEN alone is served for the VBUS management function.

## 6. Descriptor

### 6.1 Device Descriptor

Field	Size (Byte)	USB2.0 mode		Remarks
		High-Speed	Full-Speed	
bLength	1	12h	12h	
bDescriptorType	1	01h	01h	
bcdUSB	2	0200h	0200h	
bDeviceClass	1	09h	09h	
bDeviceSubClass	1	00h	00h	
bDeviceProtocol	1	01h	00h	
bMaxPacketSize0	1	40h	40h	
idVendor	2	04B8h	04B8h	EPSON
idProduct	2	0910h	0910h	S2R72A54
bcdDevice	2	0090h	0090h	
iManufacturer	1	00h	00h	
iProduct	1	00h	00h	
iSerialNumber	1	00h	00h	
bNumConfigurations	1	01h	01h	

### 6.2 Device Qualifier Descriptor

Field	Size (Byte)	USB2.0 mode		Remarks
		High-Speed	Full-Speed	
bLength	1	0Ah	0Ah	
bDescriptorType	1	06h	06h	
bcdUSB	2	0200h	0200h	
bDeviceClass	1	09h	09h	
bDeviceSubClass	1	00h	00h	
bDeviceProtocol	1	00h	01h	
bMaxPacketSize0	1	40h	40h	
bNumConfigurations	1	01h	01h	
bReserved	1	00h	00h	

## 6. Descriptor

### 6.3 Configuration Descriptor

Field	Size	USB2.0 mode		Remarks
	(Byte)	High-Speed	Full-Speed	
<b>Configuration Descriptor</b>				
bLength	1	09h	09h	
bDescriptorType	1	02h	02h	
wTotalLength	2	0019h	0019h	
bNumInterface	1	01h	01h	
bConfigurationValue	1	01h	01h	
iConfiguration	1	00h	00h	
bmAttribute	1	E0h	E0h	
bMaxPower	1	32h	32h	
<b>Interface Descriptor</b>				
bLength	1	09h	09h	
bDescriptorType	1	04h	04h	
bInterfaceNumber	1	00h	00h	
bAlternateSetting	1	00h	00h	
bNumEndpoints	1	01h	01h	
bInterfaceClass	1	09h	09h	
bInterfaceSubClass	1	00h	00h	
bInterfaceProtocol	1	00h	00h	
iInterface	1	00h	00h	
<b>Endpoint Descriptor</b>				
bLength	1	07h	07h	
bDescriptorType	1	05h	05h	
bEndpointAddress	1	81h	81h	
bmAttribute	1	03h	03h	
wMaxPacketSize	2	0001h	0001h	
bInterval	1	0Ch	FFh	

## 6.4 Other Speed Configuration Descriptor

Field	Size	USB2.0 mode		Remarks
	(Byte)	High-Speed	Full-Speed	
<b>Other_Speed_Configuration Descriptor</b>				
bLength	1	09h	09h	
bDescriptorType	1	07h	07h	
wTotalLength	2	0019h	0019h	
bNumInterface	1	01h	01h	
bConfigurationValue	1	01h	01h	
iConfiguration	1	00h	00h	
bmAttribute	1	E0h	E0h	
bMaxPower	1	32h	32h	
<b>Interface Descriptor</b>				
bLength	1	09h	09h	
bDescriptorType	1	04h	04h	
bInterfaceNumber	1	00h	00h	
bAlternateSetting	1	00h	00h	
bNUMEndpoints	1	01h	01h	
bInterfaceClass	1	09h	09h	
bInterfaceSubClass	1	00h	00h	
bInterfaceProtocol	1	00h	00h	
iInterface	1	00h	00h	
<b>Endpoint Descriptor</b>				
bLength	1	07h	07h	
bDescriptorType	1	05h	05h	
bEndpointAddress	1	81h	81h	
bmAttribute	1	03h	03h	
wMaxPacketSize	2	0001h	0001h	
bInterval	1	FFh	0Ch	

## 6.5 HUB Class Descriptor

Field	Size	USB2.0 mode		Remarks
	(Byte)	High-Speed	Full-Speed	
bDescLength	1	09h	09h	
bDescriptorType	1	29h	29h	
bNbrPorts	1	04h	04h	
wHubCharacteristics	2	0029h/0020h	0029h/0020h	Pin settings : PMODE=High/Low
bPwrOn2PwrGood	1	32h	32h	
bHubContrCurrent	1	64h	64h	
DeviceRemovable	1	00h	00h	
PortpwrCtrlMask	1	FFh	FFh	

## 7. Request List

## 7. Request List

The S2R72A54 replies STALL for those unsupported requests which are shaded in the list.

### 7.1 Standard requests

Request	bmRequest Type	bRequest	wValue	wIndex	wLength
SET_DESCRIPTOR(DEVICE)	0x00	0x07	0x0100	0x0000	0x0012
SET_DESCRIPTOR(CONFIGURATION)	0x00	0x07	0x0200	0x0000	0x0019
SET_DESCRIPTOR(String_INDEX0)	0x00	0x07	0x0300	0x0409 or 0x0000	0x0004
SET_DESCRIPTOR(String_INDEX1)	0x00	0x07	0x0301	0x0409	(variable)
SET_DESCRIPTOR(String_INDEX2)	0x00	0x07	0x0302	0x0409	(variable)
SET_DESCRIPTOR(String_INDEX3)	0x00	0x07	0x0303	0x0409	(variable)
SET_DESCRIPTOR(String_INDEX4)	0x00	0x07	0x0304	0x0409	(variable)
SET_DESCRIPTOR(String_INDEX5)	0x00	0x07	0x0305	0x0409	(variable)
SET_DESCRIPTOR(INTERFACE)	0x00	0x07	0x0400	0x0000	0x0009
SET_DESCRIPTOR(ENDPOINT)	0x00	0x07	0x0500	0x0000	0x0007
SET_DESCRIPTOR(DEVICE_QUALIFIER)	0x00	0x07	0x0600	0x0000	0x000A
SET_DESCRIPTOR(OTHER_SPEED_CONFIGURATION)	0x00	0x07	0x0700	0x0000	0x0019
SET_DESCRIPTOR(INTERFACE_POWER)	0x00	0x07	0x0800	0x0000	0x0019
GET_DESCRIPTOR(DEVICE)	0x80	0x06	0x0100	0x0000	0x0012
GET_DESCRIPTOR(CONFIGURATION)	0x80	0x06	0x0200	0x0000	0x0019
GET_DESCRIPTOR(String_INDEX0)	0x80	0x06	0x0300	0x0409 or 0x0000	0x0004
GET_DESCRIPTOR(String_INDEX1)	0x80	0x06	0x0301	0x0409	(variable)
GET_DESCRIPTOR(String_INDEX2)	0x80	0x06	0x0302	0x0409	(variable)
GET_DESCRIPTOR(String_INDEX3)	0x80	0x06	0x0303	0x0409	(variable)
GET_DESCRIPTOR(String_INDEX4)	0x80	0x06	0x0304	0x0409	(variable)
GET_DESCRIPTOR(String_INDEX5)	0x80	0x06	0x0305	0x0409	(variable)
GET_DESCRIPTOR(INTERFACE)	0x80	0x06	0x0400	0x0000	0x0009
GET_DESCRIPTOR(ENDPOINT)	0x80	0x06	0x0500	0x0000	0x0007
GET_DESCRIPTOR(DEVICE_QUALIFIER)	0x80	0x06	0x0600	0x0000	0x000A
GET_DESCRIPTOR(OTHER_SPEED_CONFIGURATION)	0x80	0x06	0x0700	0x0000	0x0019
GET_DESCRIPTOR(INTERFACE_POWER)	0x80	0x06	0x0800	0x0000	0x0019
GET_STATUS(DEVICE)	0x80	0x00	0x0000	0x0000	0x0002
GET_STATUS(INTERFACE)	0x81	0x00	0x0000	0x0000	0x0002
GET_STATUS(ENDPOINT0)	0x82	0x00	0x0000	0x00n0 (n=0 or 8)	0x0002
GET_STATUS(ENDPOINT1)	0x82	0x00	0x0000	0x0000	0x0002
SYNCH FRAME	0x82	0x0C	0x0000	0x0000	0x0002
SET_ADDRESS()	0x00	0x05	0x00mn (m=0-7, n=0-F)	0x0000	0x0000
GET_CONFIGURATION ()	0x80	0x08	0x0000	0x0000	0x0001
SET_CONFIGURATION ()	0x00	0x09	0x000n (n=0 or 1)	0x0000	0x0000
GET_INTERFACE()	0x81	0x0A	0x0000	0x0000	0x0001
SET_INTERFACE()	0x01	0x0B	0x0000	0x0000	0x0000
SET_FEATURE(DEVICE_REMOTE_WAKEUP)	0x00	0x03	0x0001	0x0000	0x0000

## 7. Request List

CLEAR_FEATURE(DEVICE_REMOTE_WAKEUP)	0x00	0x01	0x0001	0x0000	0x0000
SET_FEATURE(ENDPOINT0 HALT)	0x02	0x03	0x0000	0x00n0 (n=0 or 8)	0x0000
CLEAR_FEATURE(ENDPOINT0 HALT)	0x02	0x01	0x0000	0x00n0 (n=0 or 8)	0x0000
SET_FEATURE(ENDPOINT1 HALT)	0x02	0x03	0x0000	0x0081	0x0000
CLEAR_FEATURE(ENDPOINT1 HALT)	0x02	0x01	0x0000	0x0081	0x0000
SET_FEATURE(TEST_J)	0x00	0x03	0x0002	0x0100	0x0000
SET_FEATURE(TEST_K)	0x00	0x03	0x0002	0x0200	0x0000
SET_FEATURE(TEST_SE0_NAK)	0x00	0x03	0x0002	0x0300	0x0000
SET_FEATURE(TEST_PACKET)	0x00	0x03	0x0002	0x0400	0x0000
SET_FEATURE(TEST_FORCE_ENABLE)	0x00	0x03	0x0002	0x0500	0x0000

### 7.2 Class-specific requests

Request	bmRequest Type	bRequest	wValue	wIndex	wLength
GetHubDescriptor()	0xA0	0x06	0x0000 or 0x2900	0x0000	0x0009
SetHubDescriptor()	0x20	0x07	0x0000 or 0x2900	0x0000	0xFFFF
GetHubStatus()	0xA0	0x00	0x0000	0x0000	0x0004
GetPortStatus(Port y)	0xA3	0x00	0x0000	0x000y	0x0004
GetBusStatus(Port y)	0xA3	0x02	0x0000	0x000y	0x0001
SetHubFeature(C_HUB_LOCAL_POWER)	0x20	0x03	0x0000	0x0000	0x0000
ClearHubFeature(C_HUB_LOCAL_POWER)	0x20	0x01	0x0000	0x0000	0x0000
SetHubFeature(C_HUB_OVER_CURRENT)	0x20	0x03	0x0001	0x0000	0x0000
ClearHubFeature(C_HUB_OVER_CURRENT)	0x20	0x01	0x0001	0x0000	0x0000
SetPortFeature(PORT_CONNECTION )	0x23	0x03	0x0000	0x000y	0x0000
ClearPortFeature(PORT_CONNECTION)	0x23	0x01	0x0000	0x000y	0x0000
SetPortFeature(PORT_ENABLE)	0x23	0x03	0x0001	0x000y	0x0000
ClearPortFeature(PORT_ENABLE)	0x23	0x01	0x0001	0x000y	0x0000
SetPortFeature(PORT_SUSPEND)	0x23	0x03	0x0002	0x000y	0x0000
ClearPortFeature(PORT_SUSPEND)	0x23	0x01	0x0002	0x000y	0x0000
SetPortFeature(PORT_RESET)	0x23	0x03	0x0004	0x000y	0x0000
ClearPortFeature(PORT_RESET)	0x23	0x01	0x0004	0x000y	0x0000
SetPortFeature(PORT_POWER)	0x23	0x03	0x0008	0x000y	0x0000
ClearPortFeature(PORT_POWER)	0x23	0x01	0x0008	0x000y	0x0000
SetPortFeature(PORT_LOW_SPEED)	0x23	0x03	0x0009	0x000y	0x0000
ClearPortFeature(PORT_LOW_SPEED)	0x23	0x01	0x0009	0x000y	0x0000
SetPortFeature(PORT_HIGH_SPEED)	0x23	0x03	0x000A	0x000y	0x0000
ClearPortFeature(PORT_HIGH_SPEED)	0x23	0x01	0x000A	0x000y	0x0000
SetPortFeature(C_PORT_CONNECTION)	0x23	0x03	0x0010	0x000y	0x0000
ClearPortFeature(C_PORT_CONNECTION)	0x23	0x01	0x0010	0x000y	0x0000
SetPortFeature(C_PORT_ENABLE)	0x23	0x03	0x0011	0x000y	0x0000
ClearPortFeature(C_PORT_ENABLE)	0x23	0x01	0x0011	0x000y	0x0000
SetPortFeature(C_PORT_SUSPEND)	0x23	0x03	0x0012	0x000y	0x0000
ClearPortFeature(C_PORT_SUSPEND)	0x23	0x01	0x0012	0x000y	0x0000
SetPortFeature(C_PORT_OVER_CURRENT)	0x23	0x03	0x0013	0x000y	0x0000
ClearPortFeature(C_PORT_OVER_CURRENT)	0x23	0x01	0x0013	0x000y	0x0000
SetPortFeature(C_PORT_RESET)	0x23	0x03	0x0014	0x000y	0x0000
ClearPortFeature(C_PORT_RESET)	0x23	0x01	0x0014	0x000y	0x0000
SetPortFeature(TEST_J)	0x23	0x03	0x0015	0x010y	0x0000



## 7. Request List

ClearPortFeature(TEST_J)	0x23	0x01	0x0015	0x010y	0x0000
SetPortFeature(TEST_K)	0x23	0x03	0x0015	0x020y	0x0000
ClearPortFeature(TEST_K)	0x23	0x01	0x0015	0x020y	0x0000
SetPortFeature(TEST_SE0_NAK)	0x23	0x03	0x0015	0x030y	0x0000
ClearPortFeature(TEST_SE0_NAK)	0x23	0x01	0x0015	0x030y	0x0000
SetPortFeature(TEST_PACKET)	0x23	0x03	0x0015	0x040y	0x0000
ClearPortFeature(TEST_PACKET)	0x23	0x01	0x0015	0x040y	0x0000
SetPortFeature(TEST_FORCE_ENABLE)	0x23	0x03	0x0015	0x050y	0x0000
ClearPortFeature(TEST_FORCE_ENABLE)	0x23	0x01	0x0015	0x050y	0x0000
SetPortFeature(PORT_INDICATOR)	0x23	0x03	0x0016	0x0*0y	0x0000
ClearPortFeature(PORT_INDICATOR)	0x23	0x01	0x0016	0x0*0y	0x0000
GetTTState()	0xA3	0x0A	0x0000	0x0001	0x08D0
ResetTT()	0x23	0x09	0x0000	0x0001	0x0000
ClearTTBuffer()	0x23	0x08	(EP No.)	0x0001	0x0000
StopTT()	0x23	0x0B	0x0000	0x0001	0x0000

\*: “y” = 1-4

## 8. Electrical Characteristics

### 8.1 Absolute maximum ratings

(V<sub>SS</sub>=0V)

Item	Code	Rating	Unit
Power supply voltage	HVDD	V <sub>SS</sub> -0.3 to 4.0	V
Input voltage	HVI	V <sub>SS</sub> -0.3 to HVDD+0.5	V
	LVI *1	V <sub>SS</sub> -0.3 to 2.35	V
Output voltage	HVO	V <sub>SS</sub> -0.3 to HVDD+0.5	V
	LVO *2	V <sub>SS</sub> -0.3 to 2.35	V
Output current/pin	I <sub>out</sub> *3	±10	mA
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

\*1: XI

\*2: XO

\*3: Except USB pins

### 8.2 Recommended operating conditions

(V<sub>SS</sub>=0V)

Item	Code	MIN	TYP	MAX	Unit
Power supply	HVDD	3.00	3.30	3.60	V
Input voltage	HVI	V <sub>SS</sub> -0.3	–	HVDD+0	V
	LVI *1	V <sub>SS</sub> -0.3	–	2.15	V
Ambient temperature	T <sub>a</sub>	-40	25	105	°C

\*1: XI

## 8. Electrical Characteristics

### 8.3 DC characteristics

#### 8.3.1 Power consumption

(V<sub>SS</sub>=0V)

Item	Code	Conditions	MIN	TYP	MAX	Unit
Power consumption *1	U0=HS, D1/D2/D3,D4=HS, Data copy from D1 to D2 and from D3 to D4. (Figure 8-1)					
Power consumption	HVDD	IHC	HVDD=3.3V, Ta=25°C	-	75	115 mA
Power supply current *2	U0=HS, D1/D2/D3,D4=HS, Data copy from D1 to D2 and from D3 to D4. (Figure 8-1)					
Power supply current	HVDD	IDDH	HVDD=3.3V, Ta=25°C	-	150	225 mA
Power supply current (standby)	Internal regulator always supplies internal power when HVDD is supplied.					
Power supply current (standby)	HVDD	IDDSH	HVDD=3.6V, Ta=105°C	-	3	6 mA
Input leakage						
Input leakage current	IL	HVDD=3.6V, Ta=105°C	-5	-	5	μA

\*1: TYP values are mean current for actual operation at recommended operating conditions (Ta = 25°C). MAX values are estimated from TYP values. Those values are correlative to “bus domination” ratio because the S2R72A54 LSI saves power consumption in the idle state.

\*2: TYP values are peak current for actual operation at recommended operating conditions (Ta = 25°C). MAX values are estimated from TYP values.

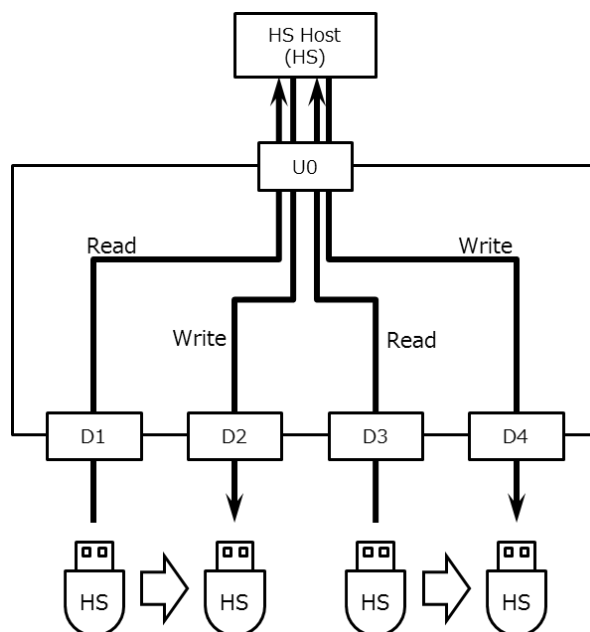


Figure 8.1 Measurement of power consumption

The operation when power consumption and power supply current is measured is shown in Figure 8.1. The HS host is connected with the U0 port, and the four HS memories are connected with the each D1/D2/D3/D4 ports. Under such condition, the file transfer of 100MB was started from D1 port to D2 port and from D3 port to D4 port. There is not connected excluding tools and materials for this evaluation in USB ports on PC used as HS host.

## 8. Electrical Characteristics

### 8.3.2 Input characteristics

(V<sub>SS</sub>=0V)

Item	Code	Conditions	MIN	TYP	MAX	Unit
Input characteristics (Schmidt)	Pins:	TESTEN, TEST0, PMODE, XRESET, U0_VBUS, D1_VBUSFLG, D2_VBUSFLG, D3_VBUSFLG, D4_VBUSFLG				
Positive trigger voltage	VT1+	HVDD = 3.3V±0.3V	1.2	-	2.52	V
Negative trigger voltage	VT1-	HVDD = 3.3V±0.3V	0.75	-	1.98	V
Hysteresis voltage	ΔV1	HVDD = 3.0V	0.30	-	-	V
Input characteristics (Clock)	Pins:	XI				
"H" level trigger voltage	VT+(XI)	HVDD = 3.3V±0.3V	-	-	1.2	V
"L" level trigger voltage	VT-(XI)	HVDD = 3.3V±0.3V	0.60	-	-	V
Input characteristics	Pins:	D1_VBUSFLG, D2_VBUSFLG, D3_VBUSFLG, D4_VBUSFLG				
Pull-up resistance	RPU1	VI = V <sub>SS</sub>	32	80	192	kΩ
Input characteristics	Pins:	TESTEN				
Pull-down resistance	RPD1	VI = HVDD	32	80	192	kΩ

(V<sub>SS</sub>=0V)

Item	Code	Conditions	MIN	TYP	MAX	Unit
USB input characteristics (FS single-ended input)	Pins:	U0_DP/U0_DM, D1_DP/D1_DM, D2_DP/D2_DM, D3_DP/D3_DM, D4_DP/D4_DM				
"H" level trigger voltage	VIH(FS)	HVDD = 3.6V	2.00	-	-	V
"L" level trigger voltage	VIL(FS)	HVDD = 3.0V	-	-	0.80	V
USB input characteristics (FS differential input)	Pins:	U0_DP/U0_DM pair, D1_DP/D1_DM pair, D2_DP/D2_DM pair, D3_DP/D3_DM pair, D4_DP/D4_DM pair				
Differential input sensitivity	VDSU	HVDD = 3.0 V Differential common mode range 0.8 V to 2.5 V	0.20	-	-	V
USB input characteristics (HS squelch)	Pins:	U0_DP/U0_DM pair, D1_DP/D1_DM pair, D2_DP/D2_DM pair, D3_DP/D3_DM pair, D4_DP/D4_DM pair				
Squelch voltage	VHSSQ	HVDD = 3.0V	100	-	200	mV
USB input characteristics (HS disconnect detection)	Pins:	D1_DP/D1_DM pair, D2_DP/D2_DM pair, D3_DP/D3_DM pair, D4_DP/D4_DM pair				
Disconnect detection voltage	VHSDSC	HVDD = 3.0V	525	-	625	mV
USB input characteristics	Pins:	U0_DP				
Pull-up resistance	RPUU	VI = V <sub>SS</sub>	1.425	-	1.575	kΩ
USB input characteristics	Pins:	D1_DP, D1_DM, D2_DP, D2_DM, D3_DP, D3_DM, D4_DP, D4_DM				
Pull-down resistance	RPDU	VI = HVDD	14.25	-	15.75	kΩ

## 8. Electrical Characteristics

### 8.3.3 Output characteristics

(V<sub>SS</sub>=0V)

Item	Code	Conditions	MIN	TYP	MAX	Unit
Output characteristics	Pins:	D1_VBUSEN, D2_VBUSEN, D3_VBUSEN, D4_VBUSEN				
“H” level output voltage	VOH1	HVDD = 3.0V IOH = -1.4mA	HVDD -0.4	-	-	V
“L” level output voltage	VOL1	HVDD = 3.0V IOL = 1.4mA	-	-	V <sub>SS</sub> +0.4	V
Output characteristics	Pins:	D1_VBUSEN, D2_VBUSEN, D3_VBUSEN, D4_VBUSEN				
Off-state leakage current	IOZ	HVDD = 3.6V VOH = HVDD VOL = V <sub>SS</sub>	-10	-	10	uA
Output characteristics (Clock)	Pins	XO				
“H” level output voltage	IOH1	HVDD = 3.0V VIH = 1.4V	-3.4	-	-1.7	mA
“L” level output voltage	IOL1	HVDD = 3.0V VIH = 0.4V	1.7	-	3.4	mA

(V<sub>SS</sub>=0V)

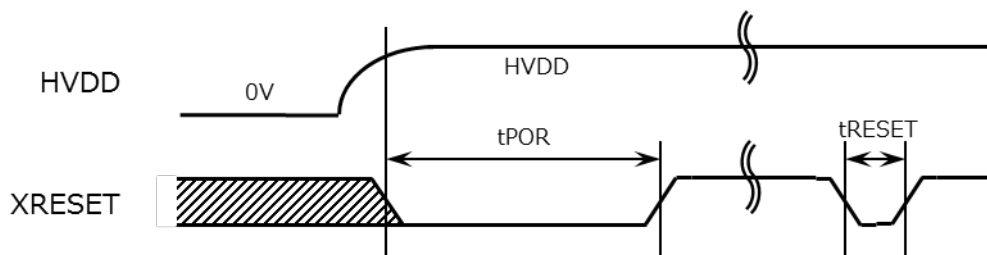
Item	Code	Conditions	MIN	TYP	MAX	Unit
USB output characteristics (HS)	Pins:	U0_DP/D0_DM, D1_DP/D1_DM, D2_DP/D2_DM, D3_DP/D3_DM, D4_DP/D4_DM				
Output current	IOUH	HVDD = 3.3V	-20	-	-18	mA
HS termination resistance (GND basis)	ROUH	HVDD = 3.3V	40.5	-	49.5	Ω
USB output characteristics (FS)	Pins:	U0_DP/D0_DM, D1_DP/D1_DM, D2_DP/D2_DM, D3_DP/D3_DM, D4_DP/D4_DM				
“H” level output voltage	VOHF	HVDD = 3.0V	2.8	-	-	V
“L” level output voltage	VOLF	HVDD = 3.6V	-	-	0.3	V
“H” level output resistance	ROHUF	HVDD = 3.3V	40.5	-	49.5	Ω
“L” level output resistance	ROLUF	HVDD = 3.3V	40.5	-	49.5	Ω

### 8.3.4 Pin capacitance

Item	Code	Conditions	MIN	TYP	MAX	Unit
Pin capacitance	Pins:	Input pins except USB				
Input pin capacitance	CI	f = 1 MHz	-	-	8	pF
Pin capacitance	Pins:	Output pins except USB				
Output pin capacitance	CO	f = 1 MHz	-	-	8	pF
Pin capacitance	Pins:	U0_DP/U0_DM, D1_DP/D1_DM, D2_DP/D2_DM, D3_DP/D3_DM, D4_DP/D4_DM				
Input/output pin capacitance (USB)	CBUH	f = 1 MHz	-	-	12	pF

8.4 AC characteristics

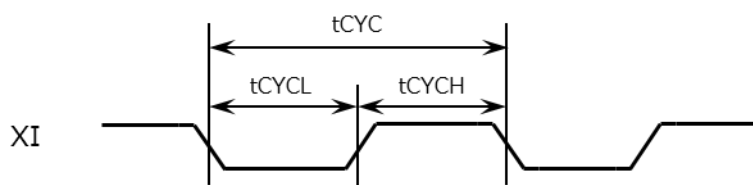
8.4.1 Reset timing



Code	Description	MIN	TYP	MAX	Unit
tPOR	Power on reset	100	–	–	us
tRESET	Reset pulse width	400	–	–	ns

\*Power-on-reset is timing from supplying more than 90% of HVDD to releasing XRESET.

8.4.2 Clock timing

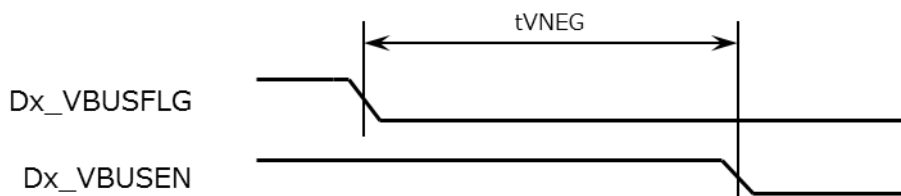


Code	Description	MIN	TYP	MAX	Unit
tCYC	Clock cycle	–	24.000	–	MHz
tCYCL tCYCH	Clock duty	–	50	–	%

8.4.3 USB I/F timing

Complies with USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard.

8.4.4 Over current detection timing



Code	Description	MIN	TYP	MAX	Unit
tvNEG	VBUSFLG assertion to VBUSEN negation time	4	–	6	ms

\*Dx = D1, D2, D3, D4

## 9. External Dimensions Diagram

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### 9. External Dimensions Diagram

#### 9.1 QFP12-48 external dimensions diagram

(Unit: mm)

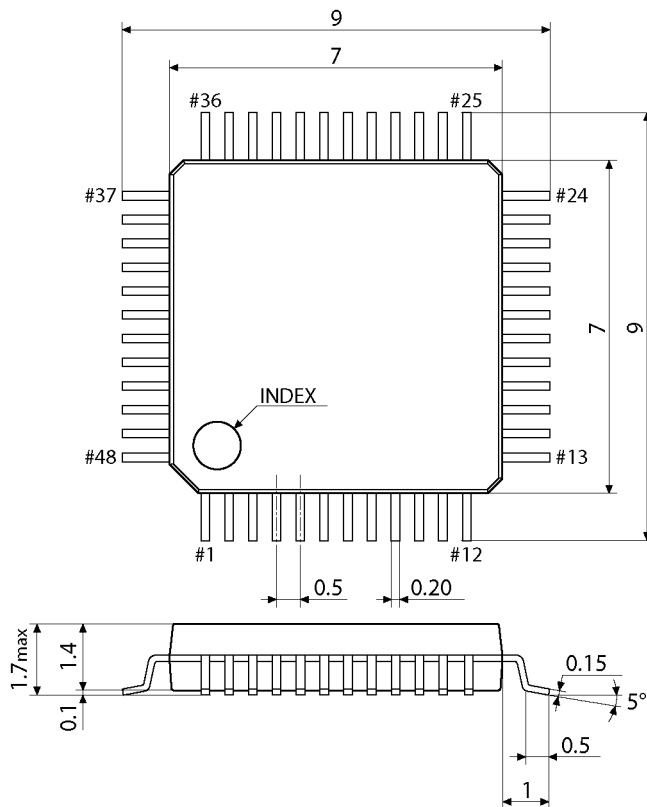
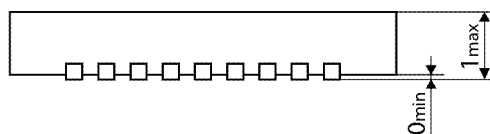
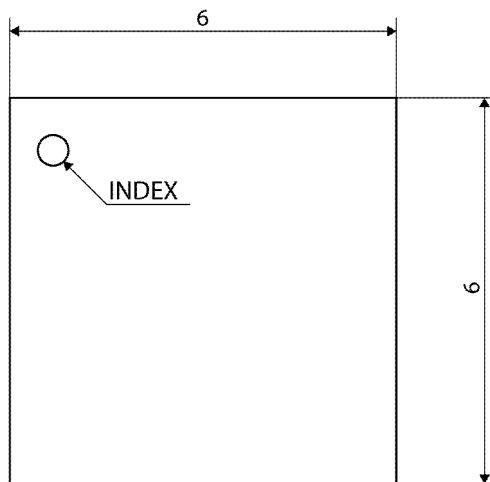


Figure 9.1 QFP12-48 external dimensions diagram

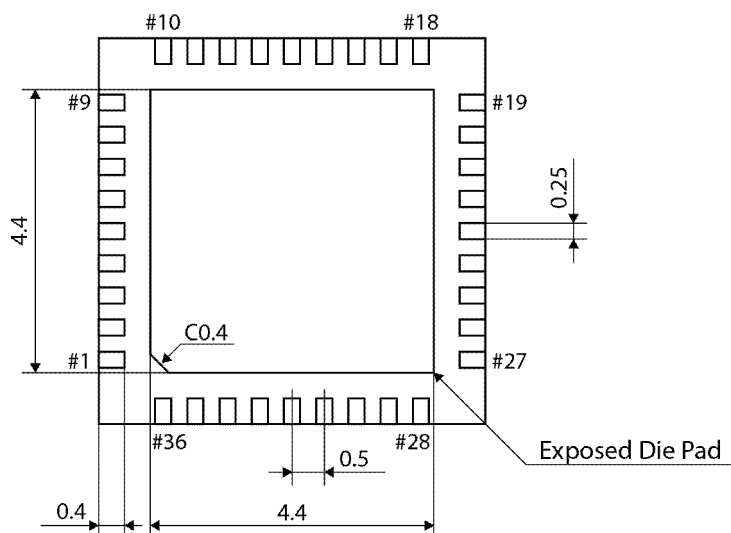
9.2 SQFN6-36 external dimensions diagram

(Unit: mm)

Top View



Bottom View



Note1: This dimension drawing may change without notification.

Note2: Exposed Die Pad has to connect to VSS on system board of customer.

Figure 9.2 SQFN6-36 external dimensions diagram

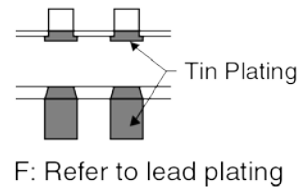
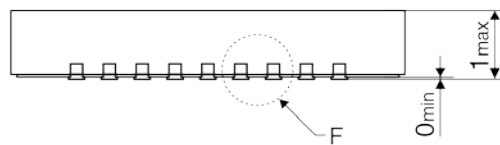
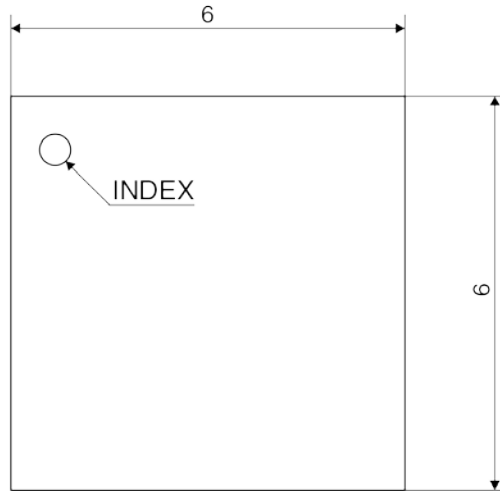


## 9. External Dimensions Diagram

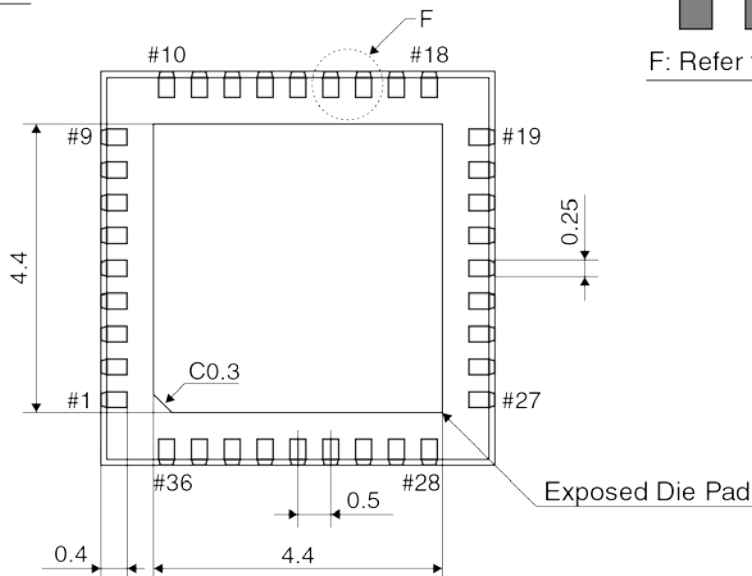
### 9.3 SQFN6-36-W external dimensions diagram

(Unit: mm)

Top View



Bottom View



Note1: This dimension drawing may change without notification.

Note2: Exposed Die Pad has to connect to VSS on system board of customer.

Figure 9.3 SQFN6-36-W external dimensions diagram

## Revision History

Attachment-1

Rev. No.	Date	Page	Type	Revision details (including previous details) and reason
Rev. 0.80	10/06/2015	All	New	New issue
Rev. 0.90	06/28/2016	P.16	Added	Added power consumption
		P.19	Added	Added power on reset timing
Rev. 1.00	10/28/2016	All	Established	Established with qualified mass production
		P. i	Added	Added configuration of product number
		P.2/4/5/20/21	Revised	Unified a name of a package and phrase of title and figure in this specification
		P.3	Revised	In Figure 3.1 Block diagram, revised from 6.2k ohm to 6.04k ohm of R1 resistor value.
		P.6	Revised	In Reference, revised from 6.2k ohm to 6.04k ohm of R1 resistor value.
		P.8	Revised	In FVDD, revised to clarify that FVDD is intermediate power to generate 1.8V.
		P.20/21	Revised	Replaced external dimensions diagram of QFP12-48 and SQFN6-36
Rev. 1.01	01/20/2017	All	Established	Re-established with qualified mass production (01/27/2017)
		P.16	Revised	In Power supply current, revised from “(static)” to “(standby)”, and from 4 mA to 6 mA of maximum current of Power supply current (standby).
		P.17	Revised	In USB input characteristics (HS squelch), revised from 150mV to 200mV that is maximum voltage.
		P.17,18	Added	Added input and output characteristics of clock pins, XI and XO.
		P.18	Revised	In USB output characteristics (HS), deleted transmission voltage and chirp voltage and showed output current and HS termination resistance only.
Rev. 1.02	02/10/2017	P.18	Revised	In output characteristics, revised IOH/IOL from -2mA/2mA to -1.4mA/1.4mA.
Rev. 1.03	31/05/2018	P.2,22	Added	Added SQFN6-36-W package.

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