S1C31D51/50 (rev2.02)

EPSON
EXCEED YOUR VISION

32-bit Single Chip Microcontroller

- Arm® 32-bit RISC CPUcore Cortex®-M0+
- Embedded 192K bytes Flash memory (Program & Sound ROM), 10K(D51)/8K(D50) bytes RAM
- Enable to output voice guidance on a buzzer in addition to a speaker
- “Voice/Audio Play"(2ch mixing play, Voice Speed Conversion w/o CPU resource)
- “Self Memory Check” w/o CPU resource

arm

■ DESCRIPTIONS

The S1C31D51/D50 is a 32-bit Arm® Cortex®-M0+ MCU which integrates a specific hardware block called the HW Processor. Normally, the buzzer does not provide sufficient voice quality and sound pressure, but our newly developed algorithm allows the buzzer to play the voice, and even devices that could not be equipped with a speaker and voice guidance can generate an error or warning, and can improve usability for the end user.
The HW Processor can perform 2ch Voice/Audio Play, Voice Speed Conversion, and Self Memory Check without using any CPU resource, and the S1C31D51/D50 is suitable for home electronics, white goods, and battery-based products which require voice and audio playback.
In addition, the audio playback format uses a high-compression, high-quality sound algorithm, which makes it possible to install multiple languages.
Furthermore, the EPSON Voice Creation PC tool makes development without studio recording easy.

■ FEATURES

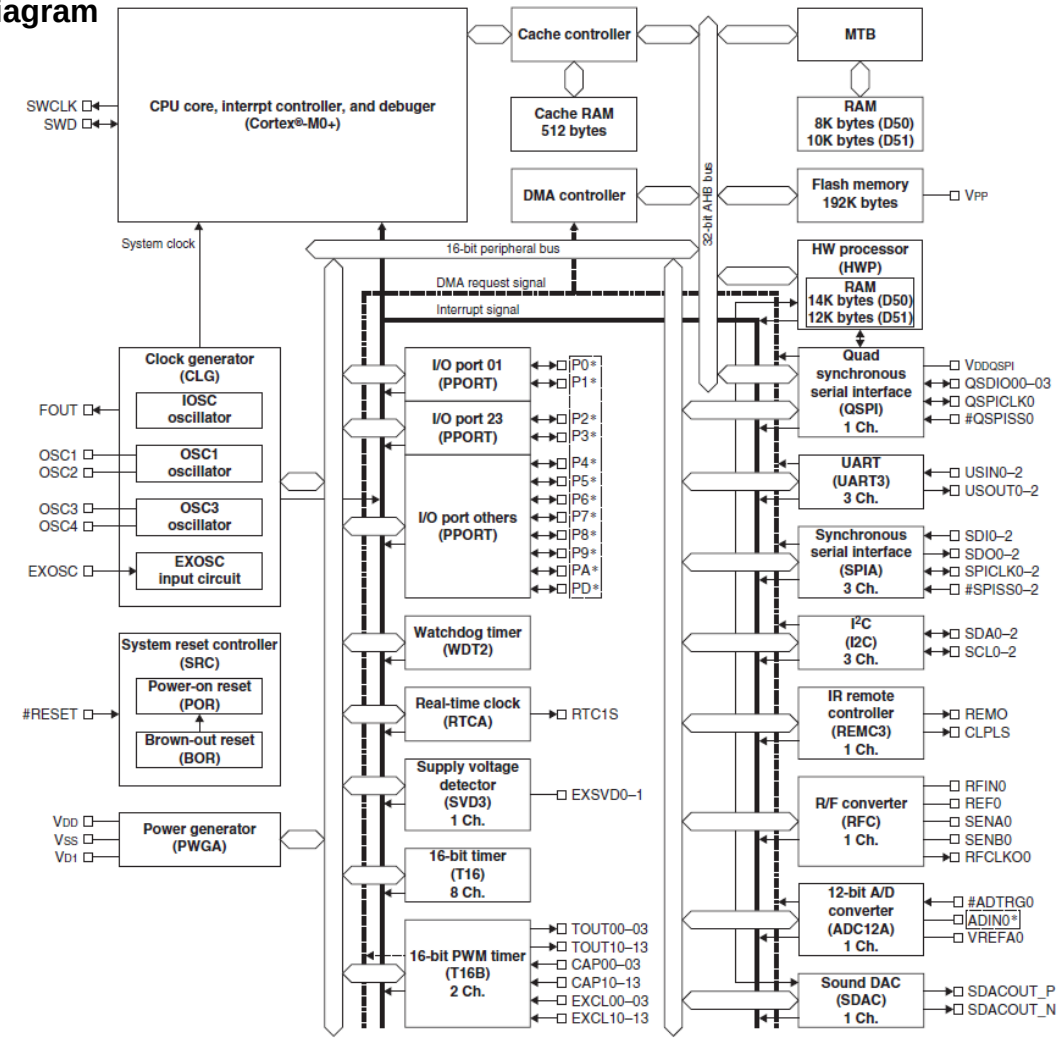
Model	S1C31D50	S1C31D51
CPU		
CPU core	Arm® 32-bit RISC CPU core Cortex®-M0+	
Other	Serial-wire debug ports (SW-DP) and a micro trace buffer (MTB) included	
Embedded Flash memory		
Capacity	192K bytes (for both instructions and data)	
Erase/program count	1,000 times (min.) * When being programmed by the dedicated flash loader	
Other	On-board programming function	
	Flash programming voltage can be generated internally.	
Embedded RAMs		
General-purpose RAM	8K bytes + 14K bytes (when HW Processor is not active)	10K bytes + 12K bytes (when HW Processor is not active)
HW Processor		
Voice Audio Play FUNCTION		
Voice/Audio Algorithm	EPSON high quality & High compress algorithm	
Play channels	2ch mixing support (example: Ch0: voice, Ch1: BGM)	
Sampling Frequency	15.625kHz, (suitable for background music + Voice play)	
Bitrate	16/24/32/40 kbps	
Voice Speed Conversion	75% - 125% (5% step)	
Self Memory Check FUNCTION		
On Chip RAM Check	W/R Check, MARCH-C	
On Chip Flash check	Checksum, CRC	
External SPI-Flash Check	Checksum, CRC	
Sound DAC		
Sampling Frequency	15.625kHz	
External Differential Circuit Speaker DAC/Electromagnetic Buzzer DAC/Piezoelectric buzzer DAC		
Sampling Frequency (A16bit PWM timer (T16B) is used)	(not supported)	**15.625kHz**
Serial interfaces		
UART (UART3)	3 channels	
	Baud-rate generator included, IrDA1.0 supported	
	Open drain output, signal polarity, and baud rate division ratio are configurable.	
	Infrared communication carrier modulation output function	
Synchronous serial interface (SPIA)	3 channels	
	2 to 16-bit variable data length	
	The 16-bit timer (T16) can be used for the baud-rate generator in master mode.	
Quad synchronous serial interface (QSPI)	1 channel	
	Supports single, dual, and quad transfer modes.	
	Low CPU overhead memory mapped access mode that can directly read data from the external flash memory with XIP (eXecute-In-Place) mode.	
I^2C (I2C)	3 channels	
	Baud-rate generator included	

Model	S1C31D50	S1C31D51
DMA Controller (DMAC)		
Number of channels	4 channels	
Data transfer bus	Memory to memory, memory to peripheral, and peripheral to memory	
Transfer mode	Basic, ping-pong, scatter-gather	
DMA trigger source	UART3, SPIA, QSPI, I2C, T16B, ADC12A, and software	
Clock generator (CLG)		
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)	
System clock frequency (operating frequency)	VD1 voltage mode = mode0: 16 MHz (max.) VD1 voltage mode = mode1: 1.8 MHz (max.)	
IOSC oscillator circuit (boot clock source)	VD1 voltage mode = mode0: 8/2/1 MHz (typ.) software selectable VD1 voltage mode = mode1: 1.9/0.9 MHz (typ.) software selectable	
	10 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)	
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator	
	32kHz (typ.) embedded oscillator	
	Oscillation stop detection circuit included	
OSC3 oscillator circuit	16 MHz (max.) crystal/ceramic oscillator	
	16/8/4MHz (typ) embedded oscillator	
EXOSC clock input	16 MHz (max.) square or sine wave input	
Other	Configurable system clock division ratio	
	Configurable system clock used at wake up from SLEEP state	
	Operating clock frequency for the CPU and all peripheral circuits is selectable.	
I/O port (PPORT)		
Number of general-purpose I/O ports	PKG48pin : 39bit(max.) PKG64pin : 55bit(max.) PKG80pin : 71bit(max.) PKG100pin : 91bit (max.)	
	Pins are shared with the peripheral I/O.	
Number of input interrupt ports	PKG48pin : 33bit(max.) PKG64pin : 49bit(max.) PKG80pin : 65bit(max.) PKG100pin : 85bit (max.)	
Number of ports that support universal port multiplexer (UPMUX)	PKG48pin : 16bit(max.) PKG64pin : 24bit(max.) PKG80pin : 27bit(max.) PKG100pin : 32bit (max.)	
	A peripheral circuit I/O function selected via software can be assigned to each port.	
Timers		
Watchdog timer (WDT2)	Generates NMI or watchdog timer reset.	
	Programmable NMI/reset generation cycle	
Real-time clock (RTCA)	128–1 Hz counter, second/minute/hour/day/day of the week/month/year counters	
	Theoretical regulation function for 1-second correction	
	Alarm and stopwatch functions	
16-bit timer (T16)	8 channels	
	Generates the SPIA and QSPI master clocks,and the ADC12A operating clock/ trigger signal.	
16-bit PWM timer (T16B)	2 channels	
	Event counter/capture function	
	PWM waveform generation function	
	Number of PWM output or capture input ports: 4 ports/channel	
Supply voltage detector (SVD3)		
Number of channels	1 channel	
Detection voltage	VDD or an external voltage (2 external detection ports are available.)	
Detection level	VDD: 28 levels (1.8 to 5.0 V)/external voltage: 32 levels (1.2 to 5.0 V)	
Other	Intermittent operation mode	
	Generates an interrupt or reset according to the detection level evaluation.	
12-bit A/D converter (ADC12A)		
Conversion method	Successive approximation type	
Resolution	12 bits	
Number of conversion channels	1 channel	
Number of analog signal inputs	8 ports/channel (max)	
R/F converter（RFC）		
Conversion method	CR oscillation type 24-bit counters	
Number of conversion channels	1 channel	
Supported sensors	DC bias resistive sensors	
IR remote controller (REMC3)		
Number of transmitter channels	1 channel	
Other	EL lamp drive waveform can be generated (by the hardware) for an application ex- ample.	
	Output inversion function	
Reset		
#RESET pin	Reset when the reset pin is set to low.	
Power-on reset	Reset at power on.	
Brown-out reset	Reset when the power supply voltage drops (when VDD ≤ 1.45 V (typ.) is detected).	
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).	
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/ disabled using a register).	

Model	S1C31D50	S1C31D51
Interrupt		
Non-maskable interrupt	6 systems (Reset, NMI, HardFault, SVCall, PendSV, SysTic)	
Programmable interrupt	External interrupt: 3 systems Internal interrupt: 27 systems	
Power supply voltage		
VDD operating voltage	1.8 to 5.5 V * If VDD > 3.6 V, the VD1 voltage mode must be mode0.	
VDD operating voltage for Flash programming	2.4 to 5.5 V (when VPP is supplied externally) 2.7 to 5.5 V (when VPP is generated internally)	
SPI-Flash interface power supply VDDQSPI	3.0 to 3.6V（possible to set main VDD:5v, SPI-Flash power supply :3.3v）	
Operating temperature		
Operating temperature range	-40 to 85 °C	
Current consumption (Typ. value)		
SLEEP mode *1	0.46 µA IOSC = OFF, OSC1 = OFF, OSC3 = OFF	
	0.95 µA IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OSC3 = OFF, RTCA = ON	
HALT mode *2	1.8 µA IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OSC3 = OFF	
RUN mode	243 µA/MHz VD1 voltage mode = mode0, CPU = OSC3 (16MHz)	
	155 µA/MHz VD1 voltage mode = mode1, CPU = IOSC (2MHz)	
Shipping form		
1	TQFP12-48PIN (P-TQFP048-0707-0.50, 7mm x 7mm, 0.5mm pitch)	
2	QFP13-64PIN (P-LQFP064-1010-0.50, 10mm x 10mm, 0.5mm pitch)	
3	TQFP14-80PIN (P-TQFP080-1212-0.50, 12mm x 12mm, 0.5mm pitch)	
4	QFP15-100PIN (P-LQFP100-1414-0.50, 14mm x 14mm, 0.5mm pitch)	

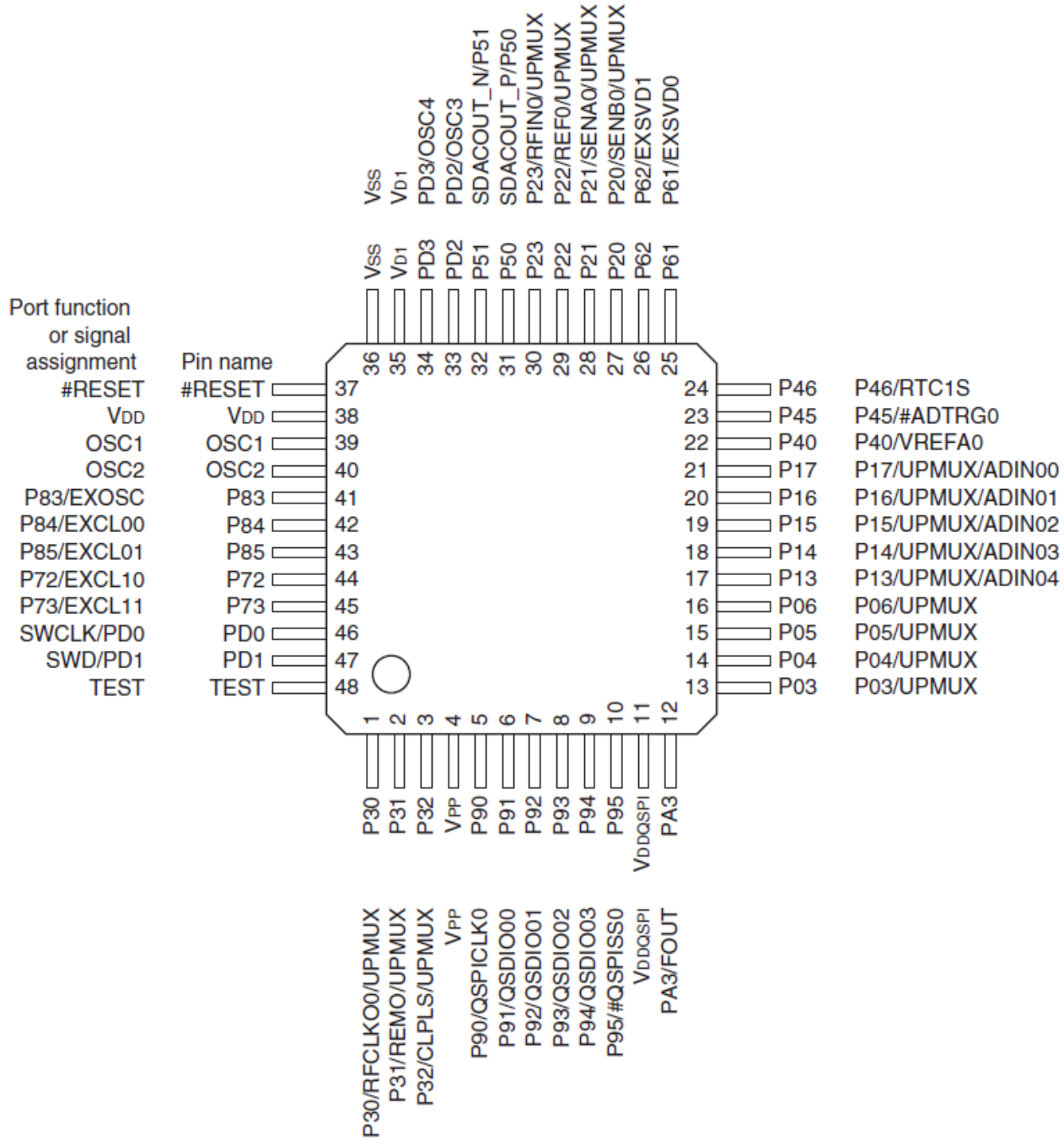
*1 SLEEP mode refers to deep sleep mode in the Cortex®-M0+ processor.
*2 HALT mode refers to sleep mode in the Cortex®-M0+ processor.

■ Block Diagram

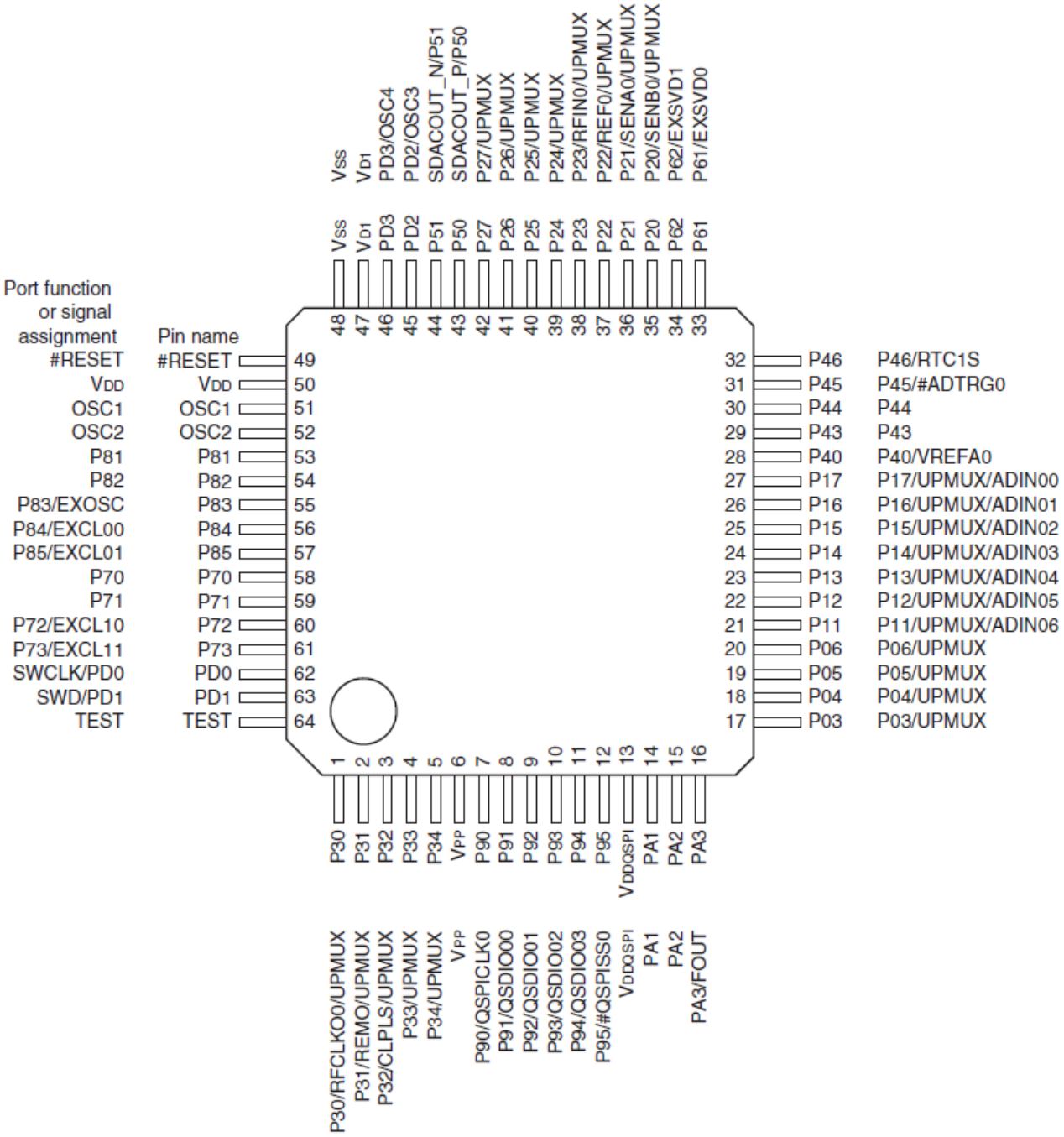


■ Pin Configuration Diagram

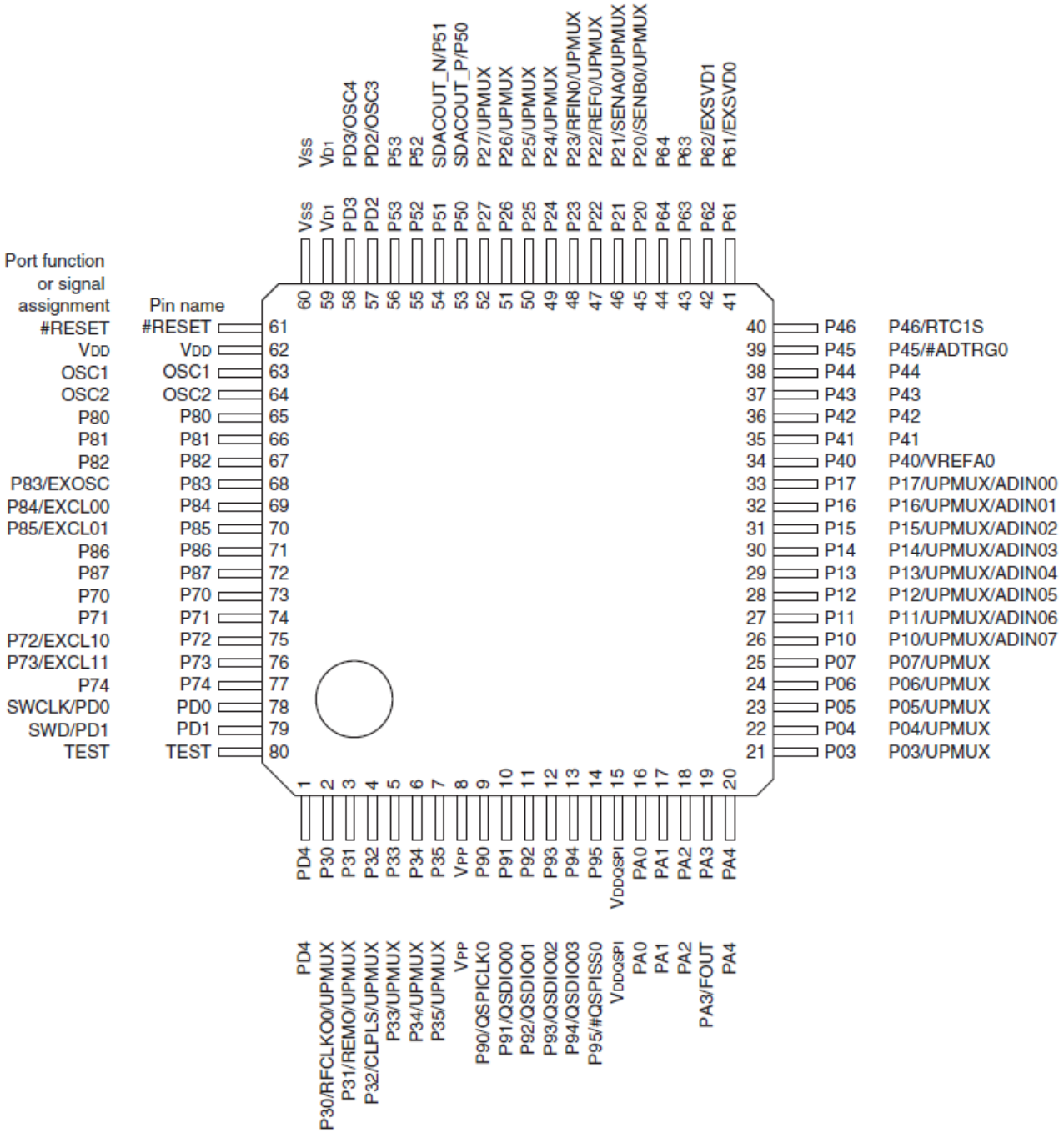
TQFP12-48



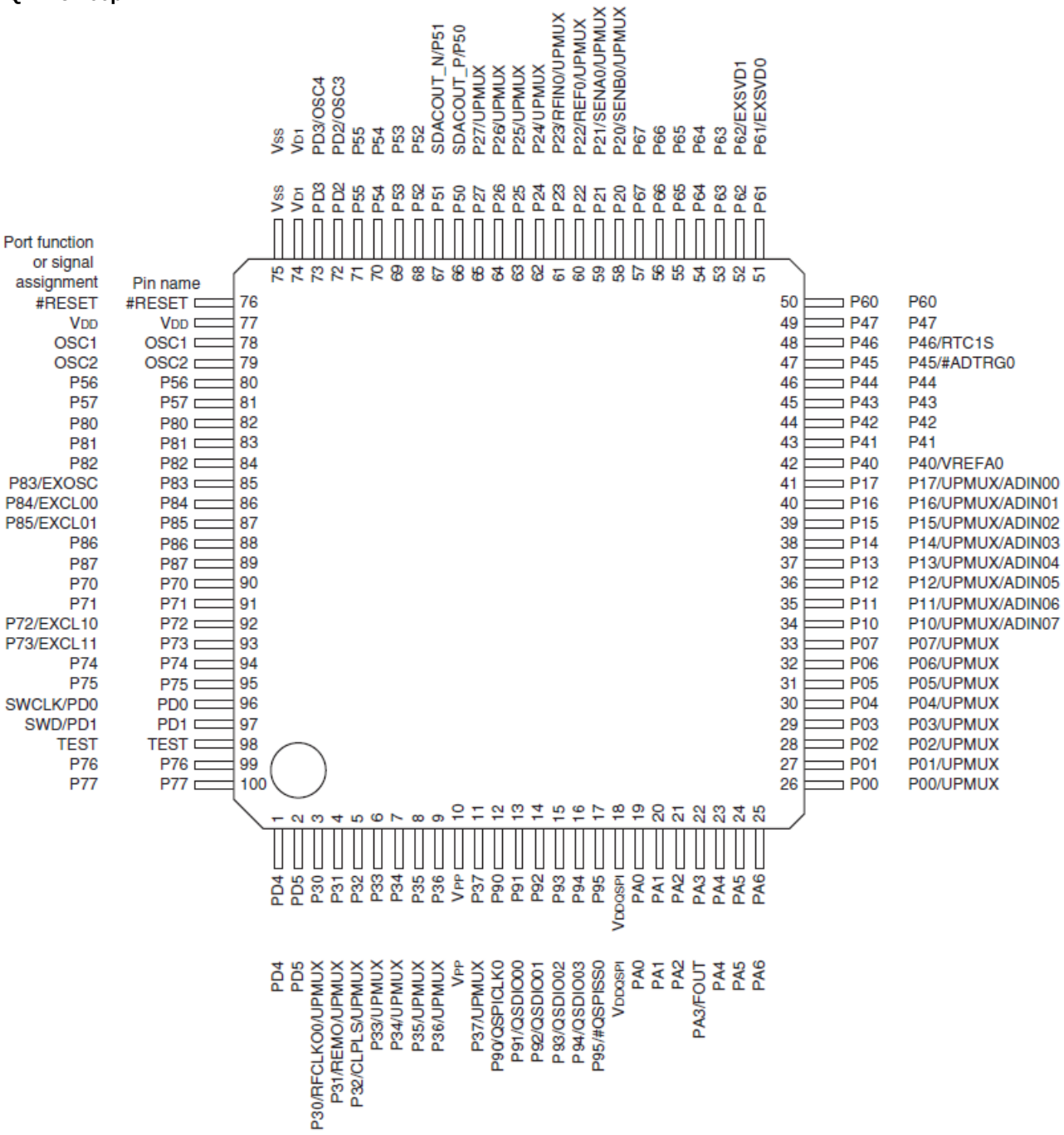
QFP13-64


Port function or signal assignment
Pin name
#RESET 49 #RESET
VDD 50 VDD
OSC1 51 OSC1
OSC2 52 OSC2
P81 53 P81
P82 54 P82
P83/EXOSC 55 P83
P84/EXCL00 56 P84
P85/EXCL01 57 P85
P70 58 P70
P71 59 P71
P72/EXCL10 60 P72
P73/EXCL11 61 P73
SWCLK/PD0 62 PD0
SWD/PD1 63 PD1
TEST 64 TEST
48 VSS
47 VD1
46 PD3
45 PD2
44 P51
43 P50
42 P27
41 P26
40 P25
39 P24
38 P23
37 P22
36 P21
35 P20
34 P62
33 P61
VSS SDACOUT_N/P51
VD1 SDACOUT_P/P50
PD3/OSC4 P27/UPMUX
PD2/OSC3 P26/UPMUX
SDACOUT_N/P51 P25/UPMUX
SDACOUT_P/P50 P24/UPMUX
P27/UPMUX P23/RFIN0/UPMUX
P26/UPMUX P22/REF0/UPMUX
P25/UPMUX P21/SENA0/UPMUX
P24/UPMUX P20/SENB0/UPMUX
P23/RFIN0/UPMUX P62/EXSVD1
P22/REF0/UPMUX P61/EXSVD0
P21/SENA0/UPMUX
P20/SENB0/UPMUX
P62/EXSVD1
P61/EXSVD0
32 P46 P46/RTC1S
31 P45 P45/#ADTRG0
30 P44 P44
29 P43 P43
28 P40 P40/VREFA0
27 P17 P17/UPMUX/ADIN00
26 P16 P16/UPMUX/ADIN01
25 P15 P15/UPMUX/ADIN02
24 P14 P14/UPMUX/ADIN03
23 P13 P13/UPMUX/ADIN04
22 P12 P12/UPMUX/ADIN05
21 P11 P11/UPMUX/ADIN06
20 P06 P06/UPMUX
19 P05 P05/UPMUX
18 P04 P04/UPMUX
17 P03 P03/UPMUX
1 P30
2 P31
3 P32
4 P33
5 P34
6 VPP
7 P90
8 P91
9 P92
10 P93
11 P94
12 P95
13 VDDQSPI
14 PA1
15 PA2
16 PA3
P30 P30/RFCLKO0/UPMUX
P31 P31/REMO/UPMUX
P32 P32/CLPLS/UPMUX
P33 P33/UPMUX
P34 P34/UPMUX
VPP VPP
P90 P90/QSPICLK0
P91 P91/QSDIO00
P92 P92/QSDIO01
P93 P93/QSDIO02
P94 P94/QSDIO03
P95 P95/#QSPISS0
VDDQSPI VDDQSPI
PA1 PA1
PA2 PA2
PA3 PA3/FOUT

TQFP14-80pin



QFP15-100pin



■ Pin Descriptions

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

I/O:	I	= Input
	O	= Output
	I/O	= Input/output
	P	= Power supply
	A	= Analog signal
	Hi-Z	= High impedance state
Initial state:	I (Pull-up)	= Input with pulled up
	I (Pull-down)	= Input with pulled down
	Hi-Z	= High impedance state
	O (H)	= High level output
	O (L)	= Low level output
Tolerant fail-safe structure:		
	✓	= Over voltage tolerant fail-safe type I/O cell included

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	Package			
						48-pin	64-pin	80-pin	100-pin
VDD	VDD	P	-	-	Power supply (+)	✓	✓	✓	✓
VSS	VSS	P	-	-	GND	✓	✓	✓	✓
VPP	VPP	P	-	-	Power supply for Flash programming	✓	✓	✓	✓
VD1	VD1	A	-	-	V_{D1} regulator output	✓	✓	✓	✓
VDDQSPI	VDDQSPI	P	-	-	QSPI interface/P9 port group power supply	✓	✓	✓	✓
OSC1	OSC1	A	-	-	OSC1 oscillator circuit input	✓	✓	✓	✓
OSC2	OSC2	A	-	-	OSC1 oscillator circuit output	✓	✓	✓	✓
TEST	TEST	I	I(Pull-down)	-	Test mode enable input	✓	✓	✓	✓
#RESET	#RESET	I	I(Pull-up)	-	Reset input	✓	✓	✓	✓
P00	P00	I/O	Hi-Z	✓	I/O port	-	-	-	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P01	P01	I/O	Hi-Z	✓	I/O port	-	-	-	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P02	P02	I/O	Hi-Z	✓	I/O port	-	-	-	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P03	P03	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P04	P04	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P05	P05	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P06	P06	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P07	P07	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P10	P10	I/O	Hi-Z	-	I/O port	-	-	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
	ADIN7	A			12-bit A/D converter Ch.0 analog signal input 7				
P11	P11	I/O	Hi-Z	-	I/O port	-	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
	ADIN6	A			12-bit A/D converter Ch.0 analog signal input 6				
P12	P12	I/O	Hi-Z	-	I/O port	-	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
	ADIN5	A			12-bit A/D converter Ch.0 analog signal input 5				
P13	P13	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
	ADIN4	A			12-bit A/D converter Ch.0 analog signal input 4				
P14	P14	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
	ADIN3	A			12-bit A/D converter Ch.0 analog signal input 3				

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	Package			
						48-pin	64-pin	80-pin	100-pin
P15	P15	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
	ADIN2	A			12-bit A/D converter Ch.0 analog signal input 2				
P16	P16	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
	ADIN1	A			12-bit A/D converter Ch.0 analog signal input 1				
P17	P17	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
	ADIN0	A			12-bit A/D converter Ch.0 analog signal input 0				
P20	P20	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	SENB0	A			R/F converter Ch.0 sensor B oscillator pin				
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P21	P21	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	SENA0	A			R/F converter Ch.0 sensor A oscillator pin				
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P22	P22	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	REF0	A			R/F converter Ch.0 reference oscillator pin				
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P23	P23	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	RFIN0	A			R/F converter Ch.0 oscillator input				
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P24	P24	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P25	P25	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P26	P26	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P27	P27	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P30	P30	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	RFCLKO0	O			R/F converter Ch.0 clock monitor output				
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P31	P31	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	REMO	O			IR remote controller transmit data output				
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P32	P32	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	CLPLS	O			IR remote controller clear pulse output				
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P33	P33	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P34	P34	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P35	P35	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P36	P36	I/O	Hi-Z	✓	I/O port	-	-	-	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P37	P37	I/O	Hi-Z	✓	I/O port	-	-	-	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)				
P40	P40	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓
	VREFA	A			12-bit A/D converter Ch.0 reference voltage input				
P41	P41	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
P42	P42	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
P43	P43	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
P44	P44	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
P45	P45	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	#ADTRG	I			12-bit A/D converter Ch.0 trigger input				
P46	P46	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	RTC1S	O			Real-time clock 1-second cycle pulse output				
P47	P47	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P50	SDACOUT_P	I/O	O(L)	✓	Sound DAC positive output	✓	✓	✓	✓
	P50				I/O port				
P51	SDACOUT_N	I/O	O(L)	✓	Sound DAC negative output	✓	✓	✓	✓
	P51				I/O port				
P52	P52	I/O	Hi-Z	✓	I/O port	-	-	✓	✓

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	Package			
						48-pin	64-pin	80-pin	100-pin
P53	P53	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
P54	P54	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P55	P55	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P56	P56	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P57	P57	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P60	P60	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P61	P61	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	EXSVD0	A			Supply voltage detector external voltage detection input 0				
P62	P62	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	EXSVD1	A			Supply voltage detector external voltage detection input 1				
P63	P63	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
P64	P64	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
P65	P65	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P66	P66	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P67	P67	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P70	P70	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
P71	P71	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
P72	P72	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	EXCL10	I			16-bit PWM timer Ch.1 event counter input 0				
P73	P73	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1				
P74	P74	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
P75	P75	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P76	P76	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P77	P77	I/O	Hi-Z	✓	I/O port	-	-	-	✓
P80	P80	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
P81	P81	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
P82	P82	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
P83	P83	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	EXOSC	I			Clock generator external clock input				
P84	P84	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	EXCL00	I			16-bit PWM timer Ch.0 event counter input 0				
P85	P85	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	EXCL01	I			16-bit PWM timer Ch.0 event counter input 1				
P86	P86	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
P87	P87	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
P90	P90	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	QSPICLK0	I/O			Quad synchronous serial interface Ch.0 clock input/output				
P91	P91	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	QSDIO00	I/O			Quad synchronous serial interface Ch.0 data input/output				
P92	P92	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	QSDIO01	I/O			Quad synchronous serial interface Ch.0 data input/output				
P93	P93	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	QSDIO02	I/O			Quad synchronous serial interface Ch.0 data input/output				
P94	P94	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	QSDIO03	I/O			Quad synchronous serial interface Ch.0 data input/output				
P95	P95	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	#QSPISS0	I/O			Quad synchronous serial interface Ch.0 slave-select input/output				

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	Package			
						48-pin	64-pin	80-pin	100-pin
PA0	PA0	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
PA1	PA1	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
PA2	PA2	I/O	Hi-Z	✓	I/O port	-	✓	✓	✓
PA3	PA3	I/O	Hi-Z	✓	I/O port	✓	✓	✓	✓
	FOUT	O			Clock external output				
PA4	PA4	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
PA5	PA5	I/O	Hi-Z	✓	I/O port	-	-	-	✓
PA6	PA6	I/O	Hi-Z	✓	I/O port	-	-	-	✓
PD0	SWCLK	I	Hi-Z	✓	Serial-wire debugger clock input	✓	✓	✓	✓
	PD0	I/O			I/O port				
PD1	SWD	I/O	Hi-Z	✓	Serial-wire debugger data input/output	✓	✓	✓	✓
	PD1	I/O			I/O port				
PD2	PD2	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓
	OSC3	A			OSC3 oscillator circuit input				
PD3	PD3	I/O	Hi-Z	-	I/O port	✓	✓	✓	✓
	OSC4	A			OSC3 oscillator circuit output				
PD4	PD4	I/O	Hi-Z	✓	I/O port	-	-	✓	✓
PD5	PD5	I/O	Hi-Z	✓	I/O port	-	-	-	✓

Universal port multiplexer (UPMUX)

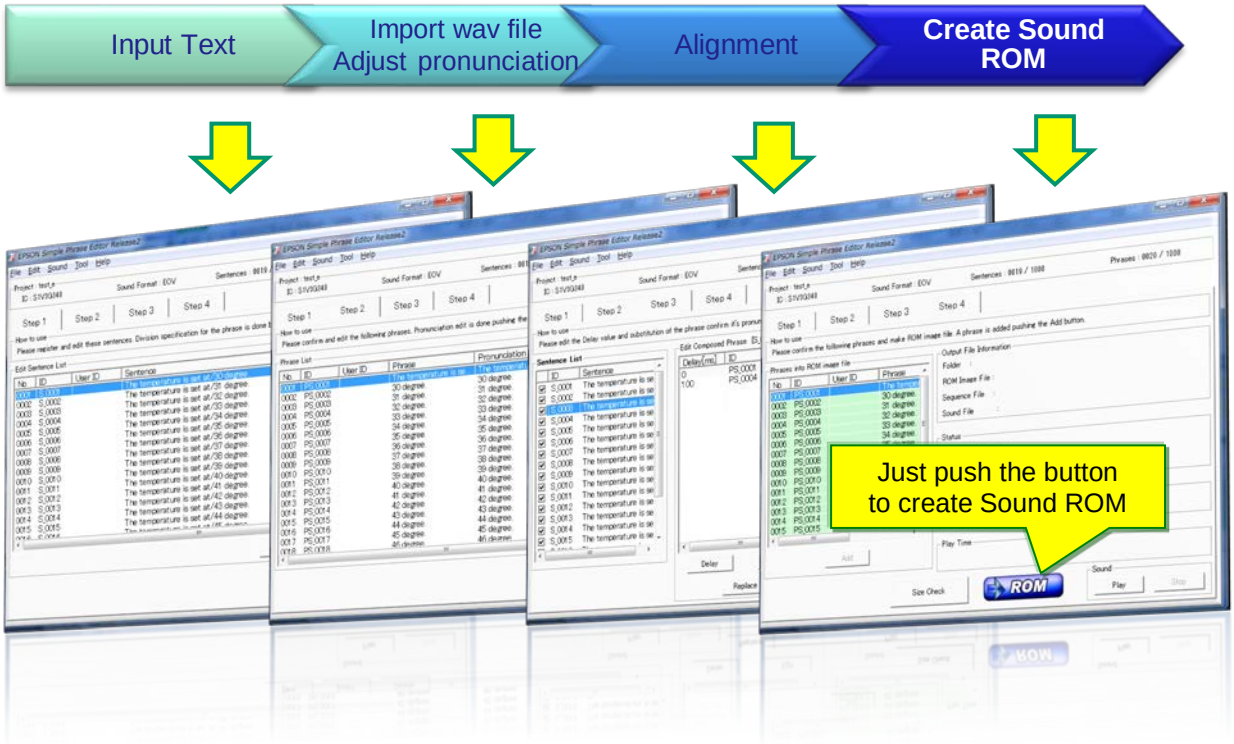
The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

Peripheral circuit	Signal to be assigned	I/O	Channel number n	Function
I^2C (I2C)	SCLn	I/O	n=0,1,2	I2C Ch.n clock input/output
	SDAn	I/O		I2C Ch.n data input/output
UART (UART3)	USINn	I	n=0,1,2	UART Ch.n data input
	USOUTn	O		UART Ch.n data output
Synchronous serial interface (SPIA)	SDIn	I	n=0,1,2	SPIA Ch.n data input
	SDOn	O		SPIA Ch.n data output
	SPICLKn	I/O		SPIA Ch.n clock input/output
	#SPISSn	I		SPIA Ch.n slave-select input
16-bit PWM timer (T16B)	TOUTn0/CAPn0	I/O	n=0,1	T16B Ch.n PWM output/capture input 0
	TOUTn1/CAPn1	I/O		T16B Ch.n PWM output/capture input 1
	TOUTn2/CAPn2	I/O		T16B Ch.n PWM output/capture input 2
	TOUTn3/CAPn3	I/O		T16B Ch.n PWM output/capture input 3

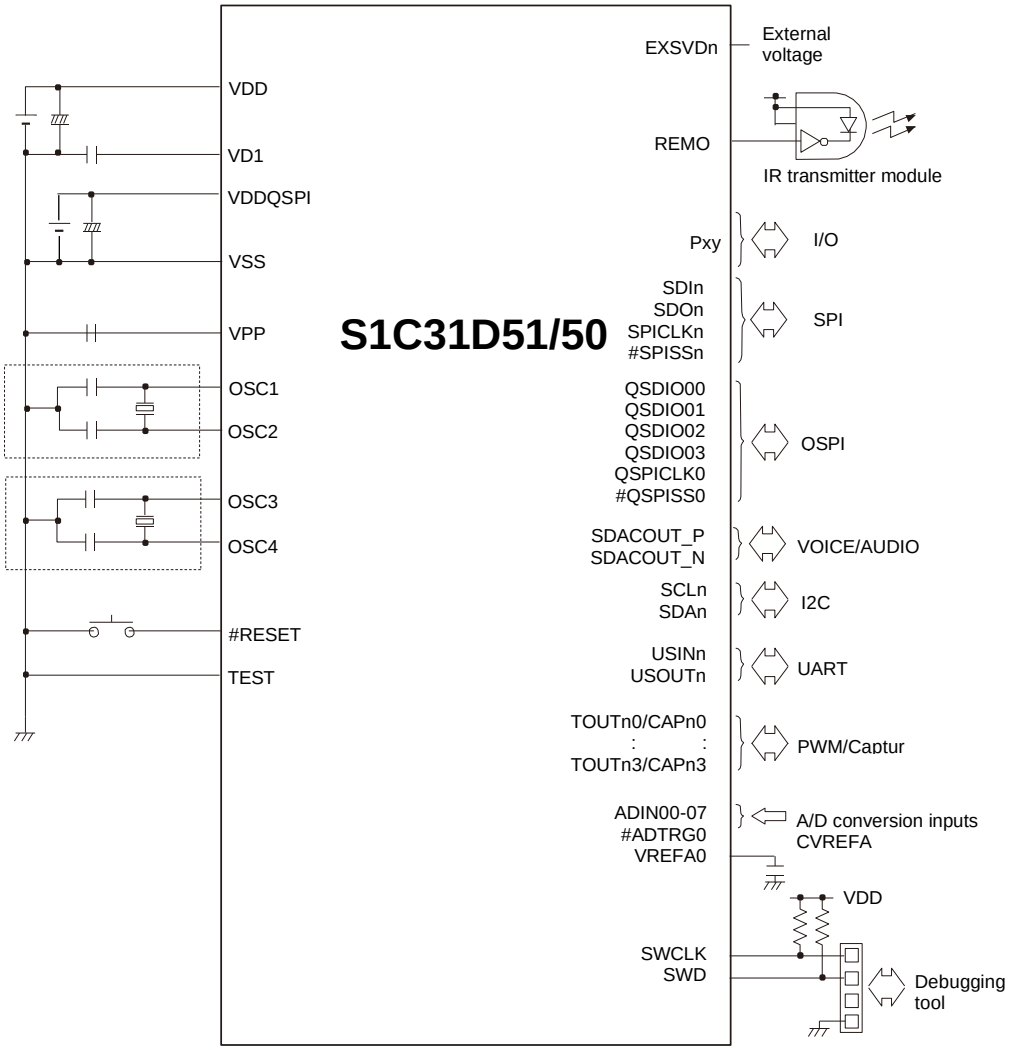
■ EPSON Voice Creation PC Tool

EPSON Voice creation PC tool makes voice related development easy because of no-studio recording, no narrator arrangement. This tool supports languages in the table below (all female voice), and easily creation, modification can be done, by “wav file” import function, existing wav file can be used.

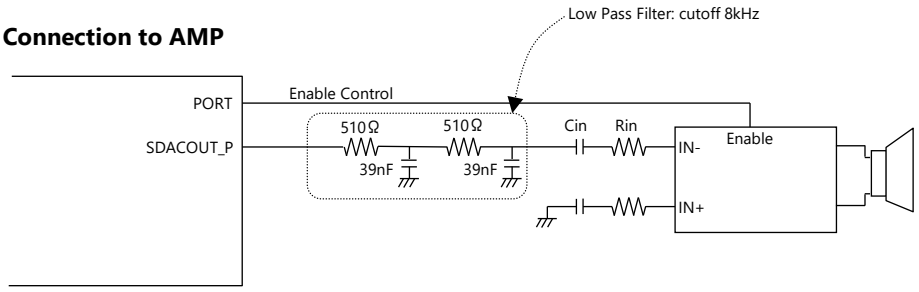
Asia	America	Europe
Chinese	American English	British English
Japanese	American Spanish	German
Korean	Canadian French	French
—	—	Spanish
—	—	Italian
—	—	Russian



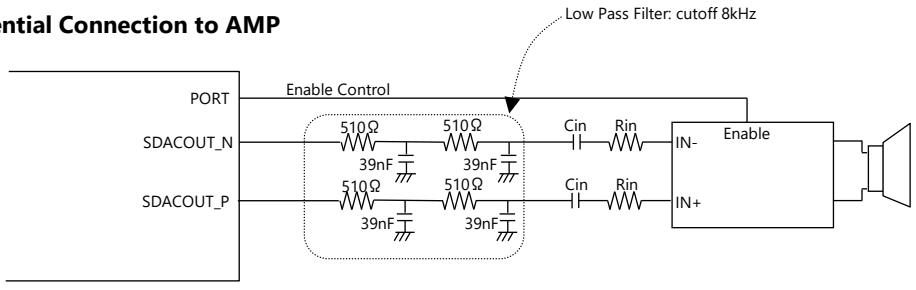
■ Basic External Connection Diagram



Single Connection to AMP



Differential Connection to AMP



■ Revision History

Date	Revision details			
	Rev.	Page	Type	Details
2018/7/30	1.00	All	New	New release
2020/6/30	2.00	All	Changed	Added S1C31D51
2020/12/15	2.01	All	Changed	Deleted "FEAUTURES" – Embedded RAMS – Instruction cache Modified "Basic External Connection Diagram"
2020/2/15	2.02	p.13	Changed	Corrected "Basic External Connection Diagram"

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