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Gate Array

S1L5V000 Series
Design Guide

SEIKO EPSON CORPORATION

Rev. 3.1

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NOTICE

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Chapter 1 Overview

The S1L5V000 Series gate arrays are fabricated on a 0.35µm process with a sea-of-gates architecture.

1.1 Features

- Process — 0.35µm CMOS, 2-, 3-, and 4-layer interconnects
- Maximum gate count — 479,988 (2-input NAND gates)
- Operating speed
  - Internal logic gates: 190ps (5.0V, typical conditions)
    290ps (3.3V, typical conditions)
    (2-input power NAND, F/O = 2, typical wire load capacitance)
  - Input buffers: 450ps (5.0V, typical conditions)
    550ps (3.3V, typical conditions)
    (F/O = 2, typical wire load capacitance and conditions)
  - Output buffers: 2.07ns (5.0V Typ.)
    2.95ns (3.3V Typ.)
    (C_L = 15pF)
- I/F levels — TTL input, CMOS input/output, and LVTTL compatible
- Input modes — TTL, CMOS, LVTTL, TTL Schmitt, CMOS Schmitt, LVTTL Schmitt, and fail-safe inputs (with output disabled)
  With built-in pull-up and pull-down resistors
  (Each resistor has two resistance values.)
- Output modes — Normal, 3-state, bi-directional, and fail-safe outputs
- Output drive — I_{OL} = 0.1, 1, 3, 8, 12mA selectable (at V_{DD} = 5.0V)
  I_{OL} = 0.1, 1, 2, 6, 10mA selectable (at V_{DD} = 3.3V)
- RAM — 1-port asynchronous, 2-port asynchronous: Max. configuration: 8Kbits/module
  1-port synchronous, 2-port synchronous: Max. configuration: 8Kbits/module
- PLL — Input frequency: 5MHz to 40MHz, output frequency: 20MHz to 135MHz
  Multiplication rate: 2, 3, 4, 6, 8, 9, 10, 12, 14, 16, 18, 20, 22, 24, 26
- Power supply/ Input/output voltage — 5.0V ±0.5V, supports single power supply operation
  3.3V ±0.3V, supports single power supply operation

1.2 Master Lineup

1.2.1 Standard Master Lineup

Five different masters are available for the S1L5V000 Series. Select the master from the master list in Table 1-1-1 to suit the required gate count, number of input/output pins (including power supply pins), and packages used.

Note that the figures provided in Table 1-1-1 do not account for RAM cell embedding. If you plan to embed RAM in the circuits, please refer to "Chapter 8 RAM Specifications" for estimates. Also note that the RAM cell configuration is fixed, and it may not be possible to apply the formula from the BC count.

Table 1-1-1 S1L5V000 Series Master List

Master	Total BC Count BC_G*1	PAD Count	BC Count		Cell Utilization U (%)*2		
			Row	Column	2-LM	3-LM	4-LM
S1L5V012/5V013/5V014	8,856	48	164	54	30	60	70
S1L5V042/5V043/5V044	42,008	104	356	118	30	60	70
S1L5V112/5V113/5V114	109,250	168	575	190	30	60	70
S1L5V252/5V253/5V254	254,330	256	877	290	25	55	65
S1L5V482/5V483/5V484	479,988	308	1206	398	25	50	60

NOTE: *1: The usable BC (gate array [G/A] basic cell) count is calculated using the following formula from the total BC count (BC_G) and cell utilization (U) for each master.
Usable BC count (BC_A) estimation formula: $BC_A = BC_G \times U$
Add approximately 550 BCs to the BC count estimation here for use with our recommended test circuit.

*2: Use the cell utilization values here strictly for reference purposes. They will vary depending not just on logic size, but on the numbers of signal lines and nodes per signal.

1.2.2 Built-in PLL Master Lineup

The S1L5V000 Series includes three types of masters with built-in PLL. The masters with built-in PLL are referred to as the S1X5V000 Series. Select the master from the master list in Table 1-1-2 to suit the required gate count, number of input/output pins (including power supply pins), and packages used.

Note that the figures provided in Table 1-1-2 do not account for RAM cell embedding. If you plan to embed RAM in the circuits, please refer to "Chapter 8 RAM Specifications" for estimates. Also note that the RAM cell configuration is fixed, and it may not be possible to apply the formula from the BC count.

Table 1-1-2 Built-in PLL S1X5V000 Series Master List (5V only)

Master	Total BC Count BC_G	PAD Count	Usable BC_A count (cell utilization U%[*1])	
			3-LM	4-LM
S1X5V513/5V514	25,960	104	14,267 (55)	16,861 (65)
S1X5V523/5V524	90,276	168	49,652 (55)	58,679 (65)
S1X5V533/5V534	235,000	256	117,500 (50)	141,000 (60)

NOTE *1: Use the cell utilization values (U) here strictly for reference purposes. They will vary depending not just on logic size, but on the numbers of signal lines and nodes per signal.
Noise generated by the PLL may affect the customer's circuits. We recommend providing a dedicated PLL power supply and maintaining the power supply separate from the customer's circuits.

1.3 Electrical Characteristics and Specifications

1.3.1 Absolute Maximum Ratings

Table 1-2 Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{DD}	-0.3 to 7.0	V
Input Voltage	V_I	-0.3 to V_{DD} +0.5[*1]	V
Output Voltage	V_O	-0.3 to V_{DD} +0.5[*1]	V
Output Current/Pin	I_{OUT}	±30	mA
Storage Temperature	T_{stg}	-65 to 150	°C

NOTE: *1: For N-channel open drain bi-directional buffers, input buffers with cell names prefixed with ID, and fail-safe buffers, the maximum allowable voltage is 7.0V.

1.3.2 Recommended Operating Conditions

Table 1-3 Recommended Operating Conditions (V_{DD} = 5.0V)

(V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage	V_I	-0.3	—	V_{DD}+0.3*1	V
Ambient Temperature	T_a	-40	25	110*2	°C
Normal Input Rising Time*3	t_{r1}	—	—	50	ns
Normal Input Falling Time*3	t_{f1}	—	—	50	ns
Schmitt Input Rising Time*3	t_{r2}	—	—	5	ms
Schmitt Input Falling Time*3	t_{f2}	—	—	5	ms

NOTE: *1: For N-channel open drain bi-directional buffers and input buffers with cell names prefixed with ID, the maximum allowable voltage is 5.8V. For fail-safe cells, the maximum allowable input voltage is 5.8V. However, do not apply an external voltage exceeding the output voltage when using high level output.
*2: Temperature range recommended when T_j = -40 to +135°C
*3: Period during which the power supply voltage changes by 10 to 90%

Table 1-4 Recommended Operating Conditions (V_{DD} = 3.3V)

(V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage*4	V_{DD}	3.0	3.3	3.6	V
Input Voltage	V_I	-0.3	—	V_{DD}+0.3*1	V
Ambient Temperature	T_a	-40	25	110*2	°C
Normal Input Rising Time*3	t_{r1}	—	—	50	ns
Normal Input Falling Time*3	t_{f1}	—	—	50	ns
Schmitt Input Rising Time*3	t_{r2}	—	—	5	ms
Schmitt Input Falling Time*3	t_{f2}	—	—	5	ms

NOTE: *1: For N-channel open drain bi-directional buffers and input buffers with cell names prefixed with ID, the maximum allowable voltage is 5.8V. For fail-safe cells, the maximum allowable input voltage is 5.8V. However, do not apply an external voltage exceeding the output voltage when using high level output.
*2: Temperature range recommended when T_j = -40 to +135°C
*3: Period during which the power supply voltage changes by 10 to 90%
*4: Built-in PLL masters do not support V_{DD} = 3.3V.

1.3.3 Electrical Characteristics

Table 1-5 Electrical Characteristics

(V_{DD} = 5.0V ±0.5V, V_{SS} = 0V, T_a = -40 to 110°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-5	—	5	µA
Off State Leakage Current	I_{OZ}	—		-5	—	5	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1mA (Type S), -1mA (Type M) -3mA (Type 1), -8mA (Type 2) -12mA (Type 3) V_{DD} = Min.		V_{DD} -0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1mA (Type S), 1mA (Type M) 3mA (Type 1), 8mA (Type 2) 12mA (Type 3) V_{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V_{IH1}	CMOS level, V_{DD} = Max.		3.5	—	V_{DD} +0.3	V
Low Level Input Voltage	V_{IL1}	CMOS level, V_{DD} = Min.		-0.3	—	1.0	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		2.0	—	4.0	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.8	—	3.1	V
Hysteresis Voltage	ΔV	CMOS Schmitt		0.3	—	-	V
High Level Input Voltage	V_{IH2}	TTL level, V_{DD} = Max.		2.0	—	V_{DD} +0.3	V
Low Level Input Voltage	V_{IL2}	TTL level, V_{DD} = Min.		-0.3	—	0.8	V
High Level Input Voltage	V_{T2+}	TTL Schmitt		1.2	—	2.4	V
Low Level Input Voltage	V_{T2-}	TTL Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H2}	TTL Schmitt		0.1	—	—	V
Pull-up Resistor	P_{PU}	V_I = 0V	Type 1	30	60	150	kΩ
			Type 2	60	120	300	kΩ
Pull-down Resistor	P_{PD}	V_I = V_{DD}	Type 1	30	60	150	kΩ
			Type 2	60	120	300	kΩ
High Level Bus Hold Current	I_{BHH}	Bus hold, V_{IN} = 2.0V, V_{DD} = Min.		—	—	-75	µA
Low Level Bus Hold Current	I_{BHL}	Bus hold, V_{IN} = 0.8V, V_{DD} = Min.		—	—	30	µA
High Level Overdrive Current	I_{BHHO}	To flip bus hold V_{IN} = 0.8V V_{DD} = Max.		-550	—	—	µA
Low Level Overdrive Current	I_{BHLO}	To flip bus hold V_{IN} = 2.0V V_{DD} = Max.		330	—	—	µA
Input Pin Capacitance	C_I	f = 1MHz, V_{DD} = 0V		—	—	10	pF
Output Pin Capacitance	C_O	f = 1MHz, V_{DD} = 0V		—	—	10	pF
IO Pin Capacitance	C_{IO}	f = 1MHz, V_{DD} = 0V		—	—	10	pF

Table 1-6 Electrical Characteristics

(V_{DD} = 3.3V ±0.3V, V_{SS} = 0V, T_a = -40 to 110°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	-		-5	—	5	µA
Off State Leakage Current	I_{OZ}	-		-5	—	5	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1mA (Type S), -1mA (Type M) -2mA (Type 1), -6mA (Type 2) -10mA (Type 3) V_{DD} = Min.		V_{DD} -0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1mA (Type S), 1mA (Type M) 2mA (Type 1), 6mA (Type 2) 10mA (Type 3) V_{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V_{IH1}	LVTTL Level, V_{DD} = Max.		2.0	—	V_{DD} +0.3	V
Low Level Input Voltage	V_{IL1}	LVTTL Level, V_{DD} = Min.		-0.3	—	0.8	V
High Level Input Voltage	V_{T1+}	LVTTL Schmitt		1.1	—	2.4	V
Low Level Input Voltage	V_{T1-}	LVTTL Schmitt		0.6	—	1.8	V
Hysteresis Voltage	ΔV	LVTTL Schmitt		0.1	—	—	V
Pull-up Resistor	P_{PU}	V_I = 0V	Type 1	40	100	250	kΩ
			Type 2	80	200	500	kΩ
Pull-down Resistor	P_{PD}	V_I = V_{DD}	Type 1	40	100	250	kΩ
			Type 2	80	200	500	kΩ
High Level Bus Hold Current	I_{BHH}	Bus hold, V_{IN} = 2.0V, V_{DD} = Min.		—	—	-18	µA
Low Level Bus Hold Current	I_{BHL}	Bus hold, V_{IN} = 0.8V, V_{DD} = Min.		—	—	15	µA
High Level Overdrive Current	I_{BHHO}	To flip bus hold	V_{IN} = 0.8V V_{DD} = Max.	-350	—	—	µA
Low Level Overdrive Current	I_{BHLO}	To flip bus hold	V_{IN} = 2.0V V_{DD} = Max.	210	—	—	µA
Input Pin Capacitance	C_I	f = 1MHz, V_{DD} = 0V		—	—	10	pF
Output Pin Capacitance	C_O	f = 1MHz, V_{DD} = 0V		—	—	10	pF
IO Pin Capacitance	C_{IO}	f = 1MHz, V_{DD} = 0V		—	—	10	pF

1.3.4 Overshoot and Undershoot

Depending on usage, if the overshoot or undershoot in input waveforms to an input buffer or bi-directional buffer exceeds the maximum input voltage under the recommended operating conditions in Tables 1-3 and 1-4, overshoot and undershoot are specified within the time periods shown below.

(1) Voltage and time for which overshoot/undershoot is allowed when V_{DD} = 5.0V ±0.5V

Overshoot maximum peak voltage:	V_{DD} + 1.5V (*1)
Overshoot maximum time (*2):	50ns
Undershoot minimum peak voltage:	V_{SS} − 1.5V
Undershoot maximum time (*2):	50ns

NOTE: *1: For N-channel open drain bi-directional buffers, input buffers with cell names prefixed with “ID”, and fail-safe buffers, the maximum allowable voltage is 7.0V.
*2: Time refers to the time for which the input voltage exceeds V_{DD} or is below V_{SS}. In the cases marked (*1) above, however, it will be the time above 5.8V.

(2) Voltage and time for which overshoot/undershoot is allowed when V_{DD} = 3.3V ±0.3V

Overshoot maximum peak voltage:	V_{DD} + 1.0V (*1)
Overshoot maximum time (*2):	50ns
Undershoot minimum peak voltage:	V_{SS} − 1.0V
Undershoot maximum time (*2):	50ns

NOTE: *1: For N-channel open drain bi-directional buffers, input buffers with cell names prefixed with ID, and fail-safe buffers, the maximum allowable voltage is 7.0V.
*2: Time refers to the time for which the input voltage exceeds V_{DD} or is below V_{SS}. In the cases marked *1 above, however, it will be the time above 5.8V.

(Supplement)
In the case of waveforms with large overshoot or undershoot, confirm that the reflected wave meets the V_{IH}/V_{IL} standards for the input. Even if the earlier mentioned standards are met, malfunctions may occur if the reflected wave is within a range that does not meet V_{IH}/V_{IL} standards. (Ideally, the input waveform should be checked directly using an oscilloscope or similar device.)

1.4 Static Current

Table 1-7 Static Current

(Tj = 110°C)

Master	5.0V ±0.5V I_{DDS}*1 Max.	3.3V ±0.3V I_{DDS}*1 Max.	Unit
S1L5V012/5V013/5V014	64	48	µA
S1L5V042/5V043/5V044 S1L5V112/5V113/5V114	240	200	µA
S1L5V252/5V253/5V254	360	280	µA
S1L5V482/5V483/5V484	520	400	µA

NOTE: *1: I_{DDS}: Static current between V_{DD} and V_{SS}

*) Use the following equation to obtain approximate static current when the temperature condition is other than Tj = 110°C. (The equation is applicable only when Tj = -40 to 110°C. If Tj is between 110°C and 135°C, please contact our sales representative.)

$I_{DDS}(Tj) = I_{DDS}(Tj = 110°C) \times$ Temperature Coefficient

$$= I_{DDS}(Tj = 110°C) \times 10^{\frac{Tj-110}{60}}$$

(Example) When V_{DD} = 5.0V and Tj = 60°C, the approximate static current of S1L5V112 is obtained as follows:

$$I_{DDS}(Tj = 60°C) = I_{DDS}(Tj = 110°C) \times 10^{\frac{60-110}{60}}$$

$$= 240 \times 0.147$$

$$= 35\ (\mu A)$$

1.5 Development Flow

Shown here are the development flow including the development start order and data submission from the customer, logic synthesis and placement and routing at Epson, and the flow from test manufacture to the start of mass production.

1.5.1 Development Flow Up to Sign-off

Figure 1-1 shows the development flow up to sign-off for an RTL interface.

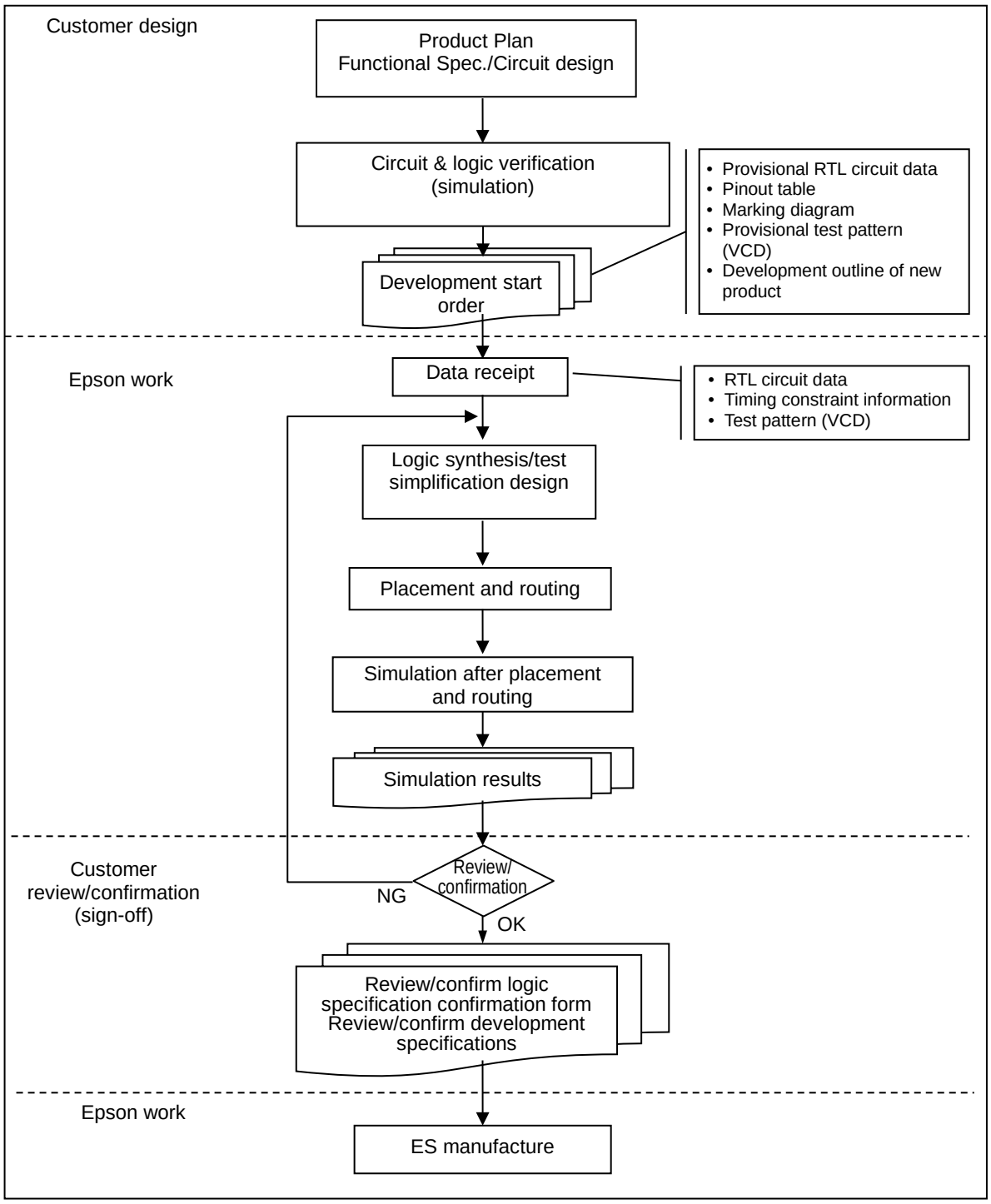


Figure 1-1 Development Flow Up to Sign-off

1.5.2 Logic Synthesis and Placement and Routing Workflow (Epson Work)

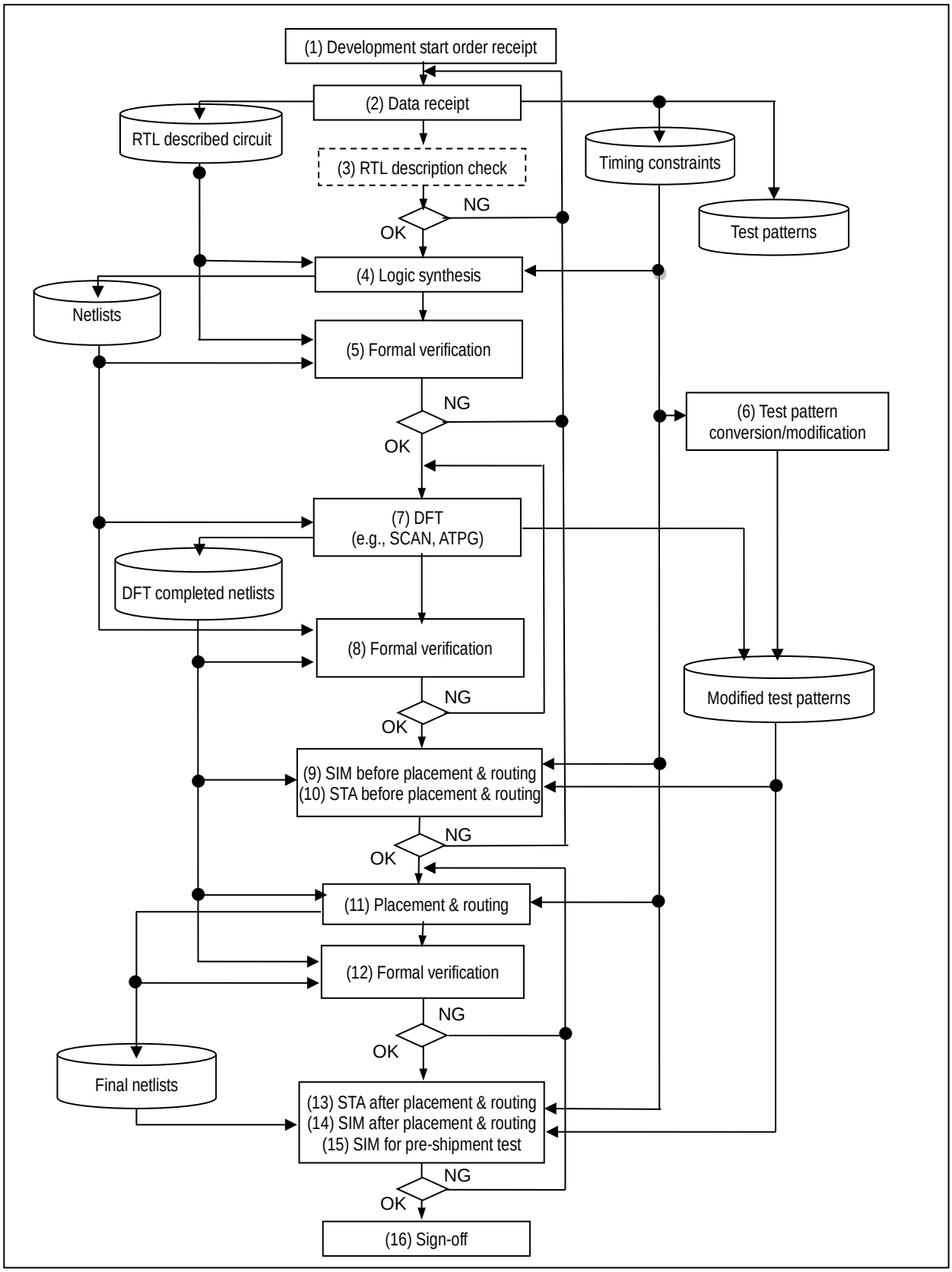


Figure 1-2 Logic Synthesis and Placement and Routing Workflow (Epson Work)

Figure 1-2 shows the logic synthesis and placement and routing workflow from data receipt to sign-off. The individual tasks are outlined as follows.

(1) Development start order receipt

The Seiko Epson development start order form is sent by the customer to Epson or to a distributor. Design work commences at Epson once this is received. The customer should also send the following data together with the development start order:

① Provisional RTL circuit data (See "1.5.3 Submitting Provisional (Trial) Data.")

② Pinout table

③ Marking diagram (form created by Epson)

④ Provisional test pattern (VCD format)

⑤ Development outline of new product

(2) Data receipt

The customer should send the following data:

① Formal RTL circuit data

② Timing constraint information

③ Test patterns (VCD format)

(3) RTL description check

An RTL checker is used as necessary to check for issues such as syntax errors.

(4) Logic synthesis

Provisional logic is synthesized initially with minimal constraints to check the number of gates and analyze the clocks. If no issues are found, the actual logic is synthesized with the addition of timing constraints.

(5) Formal verification (equivalence check)

Formal verification (equivalence check) is performed between the customer's RTL description and the netlists following logical synthesis.

(6) Test pattern conversion

VCD (value change dump) test pattern files received from the customer are converted to Epson's proprietary APF (advanced press format) files (cycle-based, table format test patterns) .

(7) DFT (e.g., scan insertion, ATPG)

DFT (design for test: addition of dedicated test circuits to increase fault coverage) is performed and scan test circuits inserted. Test patterns are generated using automatic test pattern generation (ATPG). Please inform Epson about the desired fault coverage at the start of development.

(8) Formal verification (equivalence check)

Formal verification is performed on the netlists before and after DFT.

(9) Simulation before placement and routing

Simulation is performed using the test patterns in (6) and (7) above together with virtual delay data to confirm that the required functions are achieved in the gate-level netlists. An analysis is conducted if any problems are identified in simulation results.

(10) STA before placement and routing

The timing is checked using STA (static timing analysis) based on the timing constraints received from the customer. If any clearly problematic timing errors are identified, the customer will be contacted and logic synthesis will be repeated.

(11) Placement and routing

Placement and routing is carried out using the data from (10) above. Delay time data is calculated after actual routing based on these results.

(12) Formal verification (equivalence check)

Netlists are formally verified before and after placement and routing.

(13) STA after placement and routing

The timing of the data after placement and routing is checked based on the delay time data after actual routing. If any clearly problematic timing errors are identified, adjustments will be made using ECO (local layout changes) or similar means.

(14) Simulation after placement and routing (real rate)

A simulation is performed using the data after placement and routing under the conditions using the actual IC. The results are returned to the customer for review/confirmation.

(15) Pre-shipment test simulation (test rate)

The test pattern timing conditions are modified for pre-shipment testing, then a simulation is performed using the data after placement and routing. The results are returned to the customer for review/confirmation. The customer should also confirm that the pre-shipment test conditions have been met.

<Sending simulation results>

The simulation results are sent in Seiko Epson's proprietary APF (advanced press format; *.sammax and *.sammin) . VCD (value change dump) waveform files can be sent, if requested.

<Sending comparison to simulation results>

The simulation results are compared against the expected values to output comparison files (*.exp_max and *.exp_min) . Comparison file outputs for minimum and maximum results (*.min_max) are also sent in the same way.

For an example of output, refer to "A1.1 Comparison File Example for Simulation Results and Expected Values."

<Sending timing error lists>

List (*.errmax and *.errmin) output will be sent if any timing errors occur during simulation.

For an explanation of timing error lists, refer to "A1.2 Timing Error List."

(16) Sign-off

An Epson form (logic specification confirmation form) will be sent to the customer. The customer should review the details; if no problems are found, the customer is requested to write in the confirmation results, sign and seal the form, and return it to Epson. Engineering sample (ES) manufacture will begin on receipt of this form.

1.5.3 Submitting Provisional (Trial) Data

The customer should submit provisional (trial) data before submitting formal RTL circuit data.

This provisional data is used in preparation work to ensure work proceeds smoothly following receipt of the formal data.

Please inform us when submitting provisional RTL circuit data if the timing constraints are stringent.

(1) Gate count estimate

The provisional RTL circuit data received from the customer can be used to estimate the approximate gate count.

(2) Provisional RTL data checking

The provisional RTL circuit data received from the customer is used for logic synthesis. This enables syntax and post-synthesis issues to be identified in advance. The customer will be notified of any locations where issues arose in the check.

The netlists after logic synthesis will be formally verified (equivalence checked) against the provisional RTL data. The customer will be notified if any logical inconsistencies are found.

(3) Constraint condition setting in logic synthesis

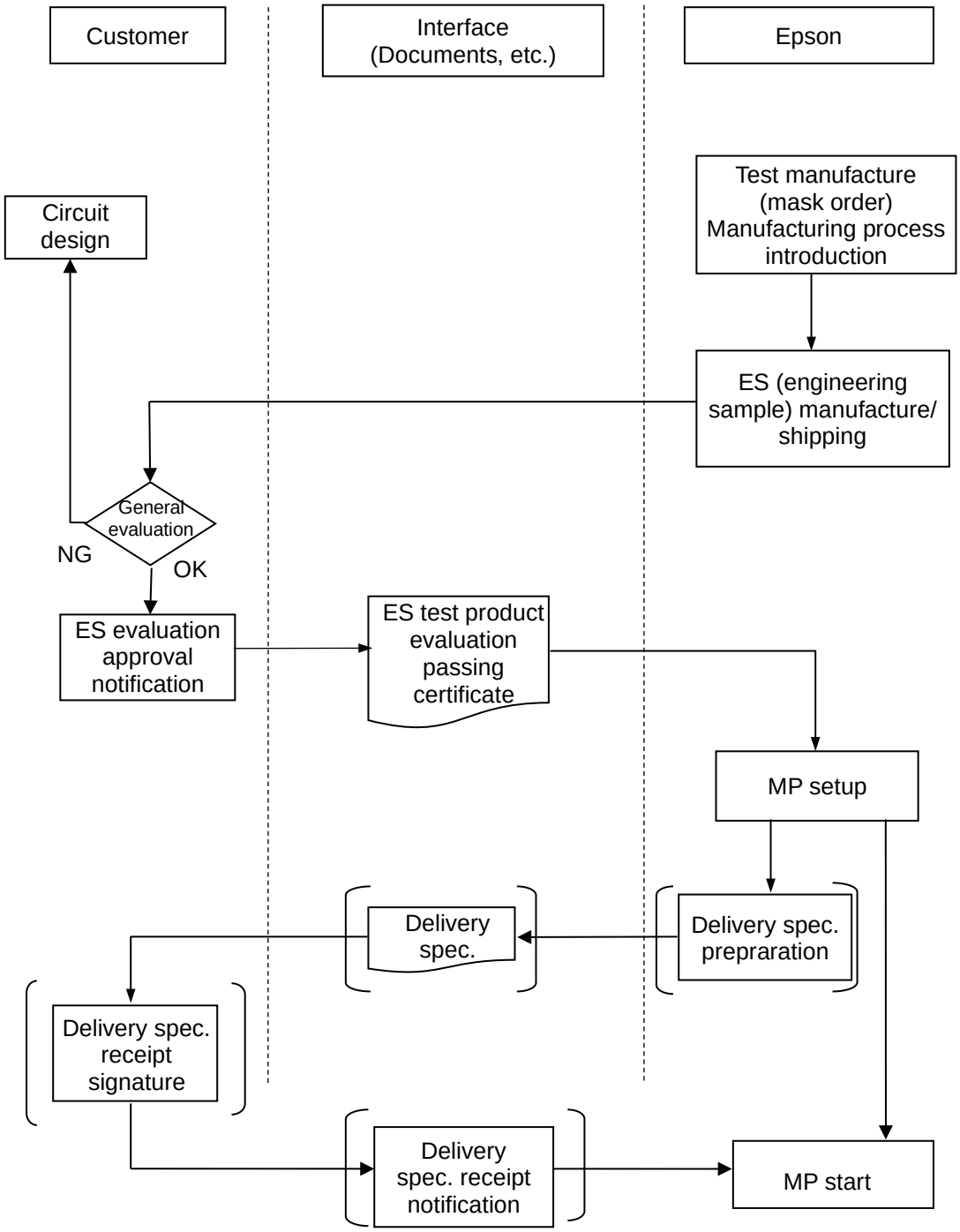
Logic synthesis is performed assuming minimal constraint conditions. Logic synthesis constraint conditions can be adjusted in advance if timing constraint information is provided by the customer. Static timing analysis (STA) constraint conditions can also be created.

(4) Function checking

If the customer provides provisional test patterns, Epson will be able to perform function checking by checking conversion to APF patterns, checking test pattern consistency, and gate level simulations.

1.5.4 Manufacturing Flow from Test Manufacture to Mass Production Setup

Figure 1-3 shows the flow from test manufacture at Epson to mass production setup.



The items in () are performed only when requested by the customer.

Figure 1-3 Flow from Test Manufacture to Mass Production Setup

Chapter 2 RTL Design Restrictions and Limitations (Verilog-HDL)

This chapter describes various precautions regarding RTL design by the customer prior to logic synthesis at Epson. The explanation here assumes use of the Verilog-HD language. Customers using VHDL should refer to "A2. RTL Design Restrictions and Limitations (VHDL)." Please inform us that the design uses VHDL when submitting the development start order.

2.1 Basic Configuration

2.1.1 Provision of RTL Data Allowing Logic Synthesis

The RTL data submitted must include only descriptions that allow logic synthesis. Logic synthesis will not be possible if behavioral-level logic is included here. Provided that it allows logic synthesis, the data may be split into multiple files.

2.1.2 Library Cell Usage

Please inform us of the names of the modules within the RTL calling up Epson library cells and the names of those library cells. Settings will be configured to ensure library cells are not deleted during logic synthesis.

2.1.3 ifdef and parameter

Please inform us if it is necessary to set values from outside the RTL or from other files for ifdef and parameter statements.

2.2 Pin Name Restrictions

The names of external and internal pins are subject to restrictions. We recommend that the customer abide by these restrictions. Please note that names that do not comply with the restrictions may be changed unexpectedly during logic synthesis.

2.2.1 External Pin Name Restrictions

(1) Describe entirely in upper case.

(2) Only alphanumeric characters and the underscore ("_") character can be used.
However, the first character must be a letter of the alphabet.

(3) Note that since square brackets "[" and "]" cannot be used, bus descriptions are prohibited.

(4) The underscore ("_") character must not be used in succession.

(5) Names must be two to 32 characters long.

2.2.2 Internal Pin Name Restrictions

(1) Names may include both upper and lower case characters. However, identical names cannot be used if they only differ by case.
Example: "ABC" and "Abc" cannot be used at the same time.

(2) Alphanumeric characters, the underscore ("_") character, and square brackets "[" and "]" for bus description can be used.

(3) Names must be two to 32 characters long.

2.2.3 Verilog Reserved Words

The following text strings are Verilog reserved words and cannot be user-defined names:

always	and	assign	begin	buf	bufif0	bufif1
case	casex	casez	cmos	deassign	default	defparam
disable	edge	else	end	endcase	endmodule	endfunction
endprimitive	endspecify	endtable	endtask	event	for	force
forever	fork	function	highz0	highz1	if	ifnone
initial	inout	input	integer	join	large	macromodule
medium	module	nand	negedge	nmos	nor	not
notif0	notif1	or	output	parameter	pmos	posedge
primitive	pull0	pull1	pullup	pulldown	rcmos	real
realtime	reg	release	repeat	rnmos	rpmos	rtranif0
rtranif1	scalared	small	specify	specparam	strong0	strong1
supply0	supply1	table	task	time	tran	tranif0
tranif1	tri	tri0	triand	trior	trireg	vectored
wait	wand	weak0	weak1	while	wire	wor
xnor	xor					

2.3 Submitting Timing Constraint Information

The customer should send timing constraint information related to clocks, input delays, and external delays at the same time as the RTL data. This information will be used for inclusion in timing constraints created for logic synthesis and STA.

2.3.1 Clock Information

(1) External clocks

Please specify the following details for all external clocks:

① Pin name

② Clock reference cycle

③ Delay from reference cycle start to clock rising edge and falling edge

④ Duty and its variation

⑤ Whether or not clock jitter is present

⑥ Whether or not skew adjustment is required

⑦ Purpose (e.g., main or test)

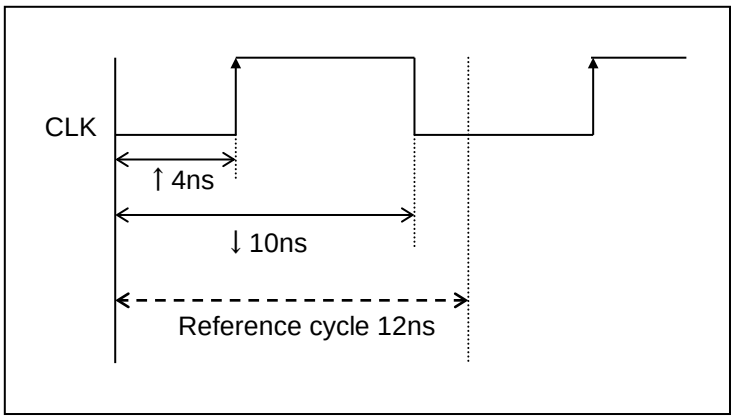


Figure 2-1 External Clock Waveform

For example, in the case shown in Figure 2-1, the external clock pin name is CLK, the clock reference cycle is 12ns, the rising edge delay is 4ns, the falling edge delay is 10ns, and duty is 50 ±0%.

(2) Internally generated clocks

This refers to clocks generated within the circuits by methods such as PLL or division. Please specify the following details for all internally generated clocks:

① Internally generated clock signal name and name of module in which it is generated

② Master clock signal name (or pin name if it is an external clock)

③ Relationship with master clock (division or multiplication rate)

④ Whether or not skew adjustment is required

Figure 2-2 shows an example RTL description generating an internal clock DCLK in which the master clock CLK is divided in two using D-FF. Following logic synthesis, this produces a circuit like that shown in Figure 2-3. Note here that CLK and DCLK will be clocks with different timings. This is because skew corresponding to the propagation delay occurs between CLK and the FF output pin. See Figure 2-4.

```
always @(posedge CLK or negedge RST)
begin
  if(!RST)
    Q <= 1'b0;
  else
    Q <= ~Q;
end

assign DCLK = Q;

always @(posedge DCLK or negedge RST)
                    .
                    .
```

Figure 2-2 Example Description for Internal Clock Generation Using Division

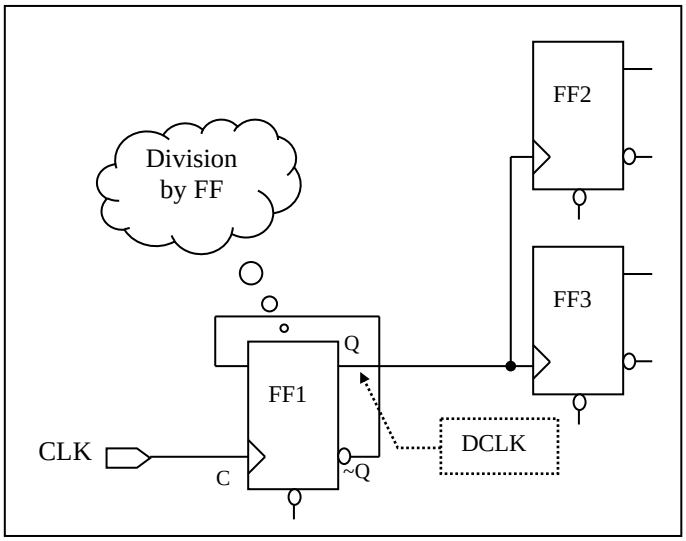


Figure 2-3 Example Circuit Synthesized from Figure 2-2

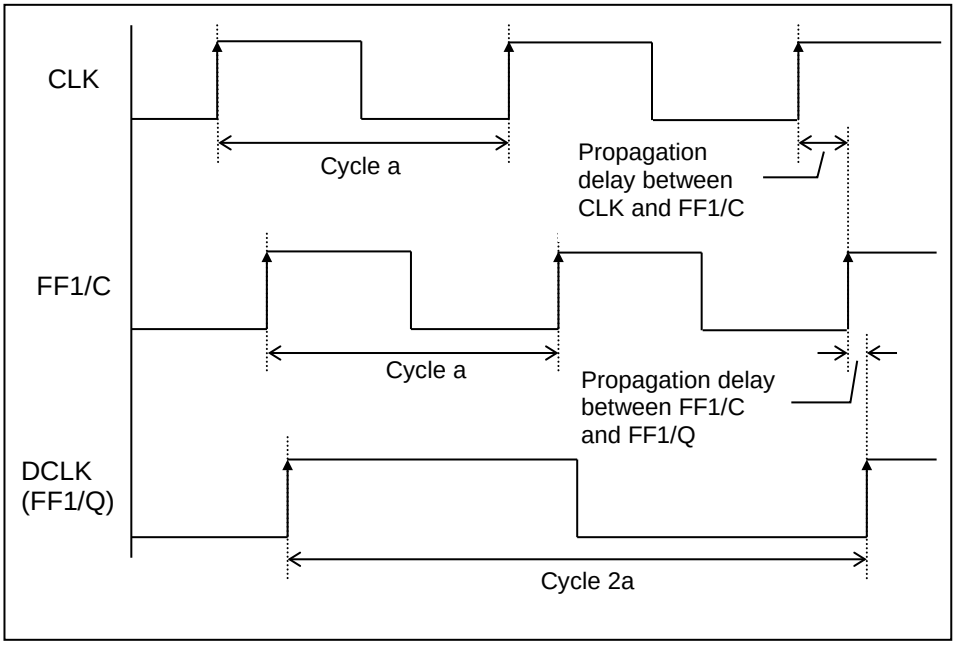


Figure 2-4 Waveform for Circuit in Figure 2-3

(3) Combining multiple clocks

Avoid generating pulses using circuits consisting of multiple clocks. The skew from each clock may result in unpredictable pulses.

(4) Data paths between registers operating using different clocks

The presence of data paths between registers operating using different clocks will make it difficult to guarantee their timing. The design should ensure that data can be received asynchronously. Likewise, in cases in which the edge differs even with the same clock, please specify whether it is acceptable to treat these registers as using different clocks.

2.3.2 External Pin Timing Constraints

(1) External input timing

Please specify the setup time and hold time with respect to the reference clock for external input pins.

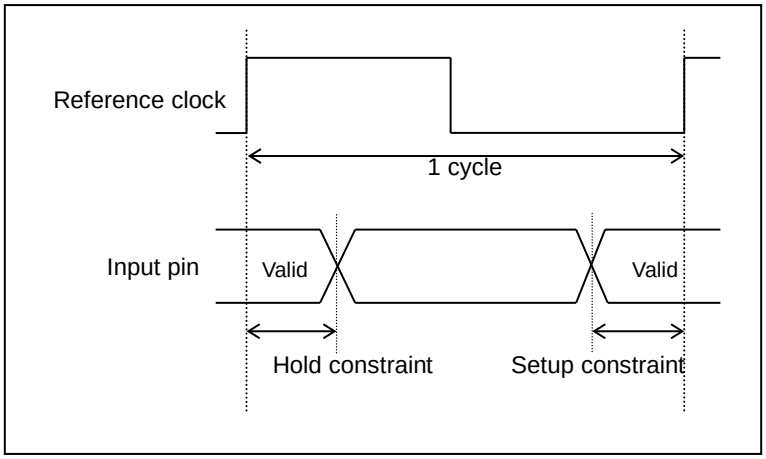


Figure 2-5 External Input Timing

(2) External output timing

Set the output delay with respect to the defined clock for external output pins. Please specify maximum and minimum delays with respect to the reference clock. Specify virtual clock constraints if the circuit lacks a reference clock.

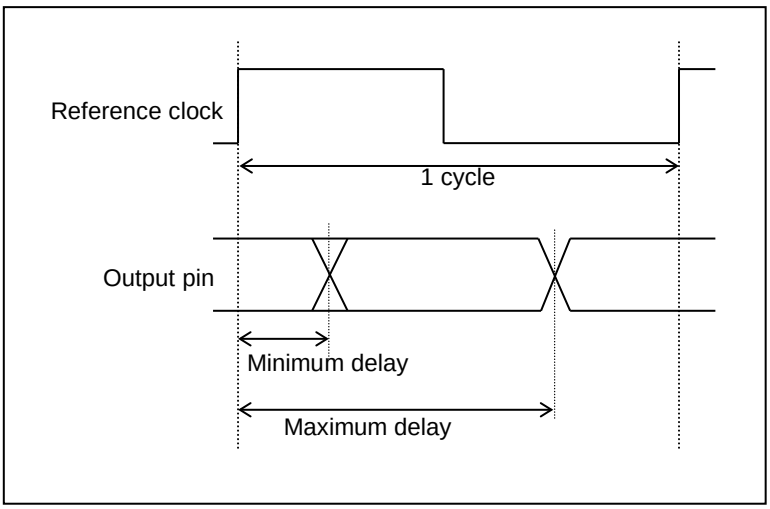


Figure 2-6 External Output Timing

(3) Multi-cycle paths

Figure 2-7 shows an example of a path through a large-scale circuit such as a multiplier. If multiple cycles are required (or the necessity of multiple cycles is allowed) for timing between FF1/Q and FF2/D, specify multi-cycle paths for paths between FF1/Q and FF2/D.

Specify the paths requiring multiple cycles for transferring data and the number of cycles.

For example, if two cycles are required for data propagation on the path between FF1/Q and FF2/D, specify a two-cycle multi-cycle path between FF1/Q and FF2/D, as shown in Figure 2-8.

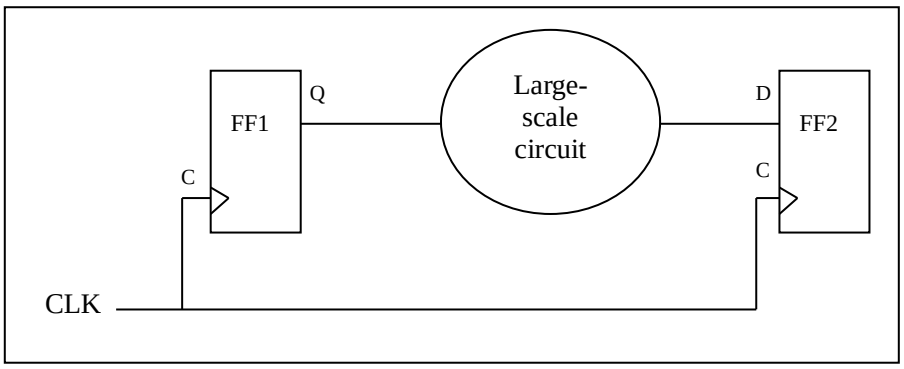


Figure 2-7 Example Path through Large-scale Circuit

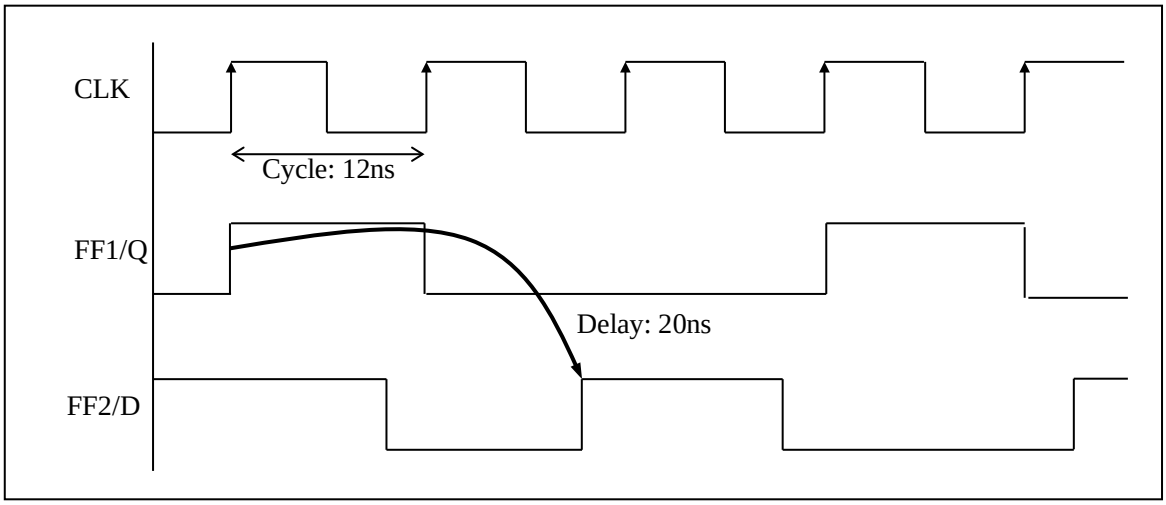


Figure 2-8 Multi-cycle Path

(4) False paths

Where possible, specify paths that are logically infeasible or fall outside specifications. False paths will be excluded from optimization. For example, the path between B and X in Figure 2-9 is logically infeasible, and therefore constitutes a false path.

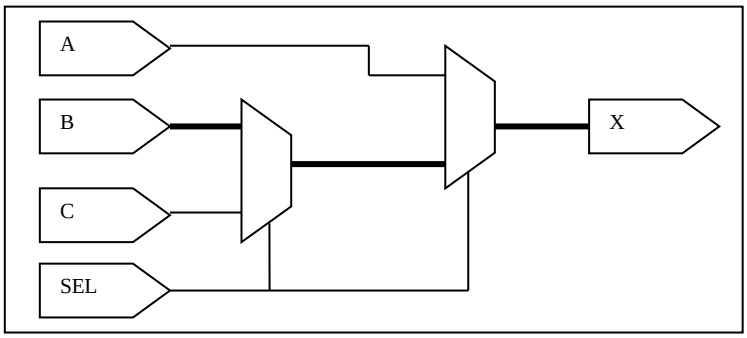


Figure 2-9 False Path

(5) Clock gating

Ideally, clock gating used to reduce power consumption should be performed at higher levels.

Please specify the locations where clock gating is performed. It may be necessary to adjust skew when constructing the clock tree. Additionally, specify if latch-based clock gating cells are used.

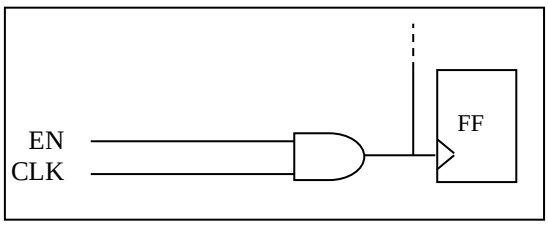


Figure 2-10 Clock Gating Example

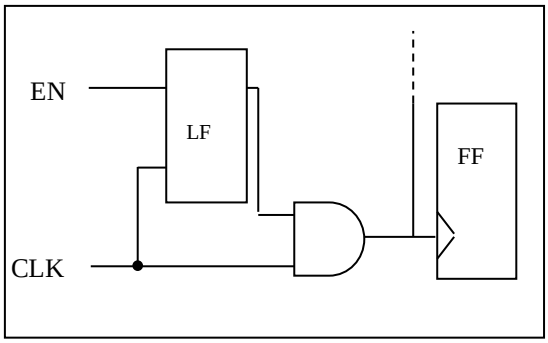


Figure 2-11 Latch-based Clock Gating Example

(6) Precautions for simulations using RTL with clock gating

In RTL simulations, clocks gated as shown in Figure 2-12 will be treated as asynchronous to the clock before gating. If a clock is input with zero delay for both two-stage asynchronous FF, the simulator will determine the one processed first. To avoid this, add a delay description within the RTL to ensure processing is carried out in the desired order. Delay descriptions within the RTL will be ignored during logical synthesis.

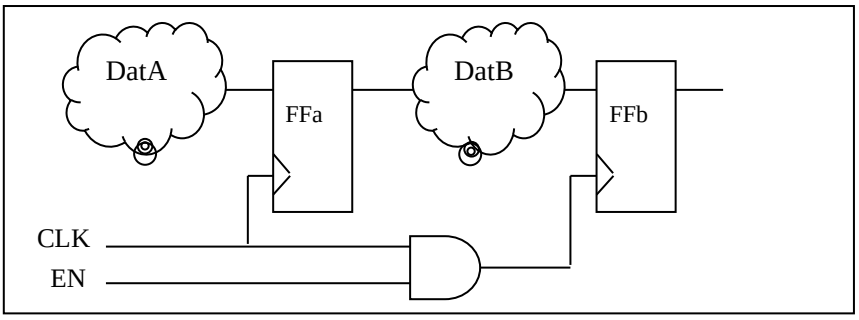


Figure 2-12 Example of Connection with Gated Clock

```
parameter DELAY = 10;
.......
always @(posedge CLK ) begin
      FFa <=   #(DELAY)   DatA;
end
assign ENCLK = CLK & EN;
always @(posedge ENCLK ) begin
      FFb <=   DatB;
end
```

Figure 2-13 Additional Delay Description

(7) Automatic clock gating cell insertion during logical synthesis

Latch-based clock gating cells can be automatically inserted during logical synthesis at Epson to reduce power consumption and gate size.

However, note that adjustment may take several days if timing constraints are stringent, due to the resulting increase in clock skew.

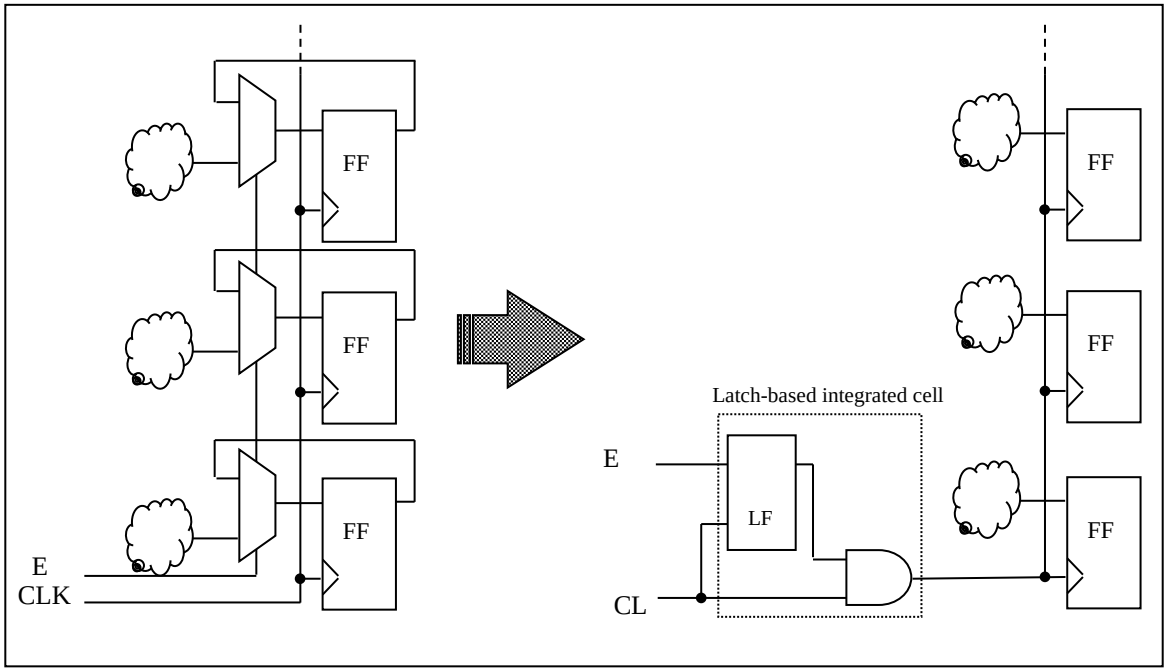


Figure 2-14 Example of Automatic Clock Gating Cell Insertion

(8) Set/reset signals

Please specify whether there are any flip-flops that have both asynchronous set and reset pins as shown in Figure 2-15. The recovery time and removal time cannot be analyzed between setting and resetting flip-flops that have both asynchronous set/reset pins. Similarly, setting/resetting cannot be analyzed for cells with no clock pins.

```
always @(posedge CLK or negedge SET or negedge RST) begin
   if (!SET)
      Q <= 1'b1;
   else if (!RST)
      Q <= 1'b0;
   else
      Q <= D;
end
```

Figure 2-15 Example Description for Flip-flop with Both Set and Reset Pins

2.4 I/O Buffer Insertion

(1) Epson will insert I/O buffers depending on the buffer types in the pinout table sent by the customer.

For information on buffer types and configurations, refer to "Chapter 6 Types of I/O Buffers and Notes on Use."

(2) I/O buffers can be inserted safely and easily by changing the top module from an RTL module to a gate module. The gate top module will be created by Epson. The customer only needs to include descriptions related to input and output in the RTL top module. More specifically, uni-directional ports should be connected only to lower modules on a one-to-one basis. The descriptions for bi-directional ports should include descriptions for bi-directional signals within the top module by extracting input signal ports, output signal ports, and enable signal ports from the lower level.

```
module TOP ( IN1, OUT1, BID1);
   input IN1;
   output OUT1;
   inout BID1;
   assign BID1 = (en) ? 1'bz : bid1_out;
   CORE U_CORE( .in1(IN1),
   .out1(OUT1), .bid1_in(BID1),
   .bid1_out(bid1_out), .en(en) );
endmodule
```

Figure 2-16 Top Module RTL Example

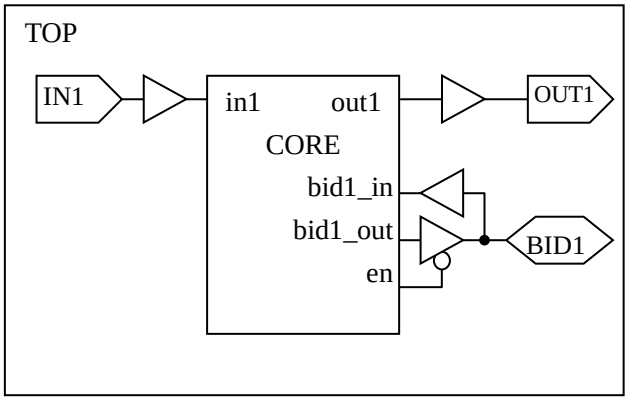


Figure 2-17 Top Module Schematic

2.5 RAM Description

(1) Please check the RAM specifications if RAM is installed. For more information on specifications, refer to "Chapter 8 RAM Specifications."

(2) Epson will provide RAM libraries. Please indicate the required RAM size and quantity in the development start order. Note that it may take several days to provide RAM (model) libraries.

(3) If RAM is described by the customer, please notify us of the model module name.

2.6 Oscillator Cell Description

(1) If oscillator cells are installed, refer to "5.1 Oscillator Circuits" for details on oscillator cells.

(2) Oscillator cells should be instantiated in the RTL description.

(3) If logic synthesis is performed by the customer, add the "dont_touch" attribute using the "set_dont_touch" command to the input and output nets to prevent buffers from being inserted into the nets connecting the external pins of the oscillator cells.

Chapter 3 Test Circuit Design Restrictions and Limitations

For test circuit design, we recommend simplified test design and test circuit insertion at Epson. For information on the insertion procedure, refer to "1.5 Development Flow."

3.1 Recommended AC/DC Test Circuit Insertion

Epson provides recommended test circuits to ensure efficient pre-shipment testing of AC and DC circuits. These will be inserted into the customer's circuits.

3.1.1 Using Recommended Test Circuits and I/O Buffers with Test Circuits

Epson-recommended AC and DC test circuits will be inserted by Epson into the circuits sent by the customer. I/O buffers with test circuits will be selected to configure the recommended test circuits.

Please provide at least one input pin for use as a dedicated AC/DC test pin.

3.1.2 Cell Names for Output Buffers with Test Circuits and Bi-directional Buffers

The cell names for output buffers with test circuits selected for configuring recommended test circuits will be "O***T" or "TB***T", and the cell names for bi-directional buffers will be "B****T", all suffixed with "T".

3.1.3 Test Circuit Insertion Designed by Customer

Please indicate in the development start order if the test circuits are designed by the customer, if Epson-recommended test circuits cannot be used for reasons involving the customer's circuit configuration, or if an output buffer with test function cannot be used.

3.2 Scan Circuit Insertion

Please indicate in the development start order whether scan circuits are to be inserted. Scan circuits will be inserted by Epson.

If so, provide two dedicated scan test pins for use as circuit input and output pins.

3.2.1 Scan Circuits

Scan insertion by Epson involves replacing all registers (D-FF and JK-FF) existing in the design created with scan-type registers, then configuring the scan paths (full-scan design) . Using auto test pattern generation (ATPG) with this design generates test patterns with high fault coverage.

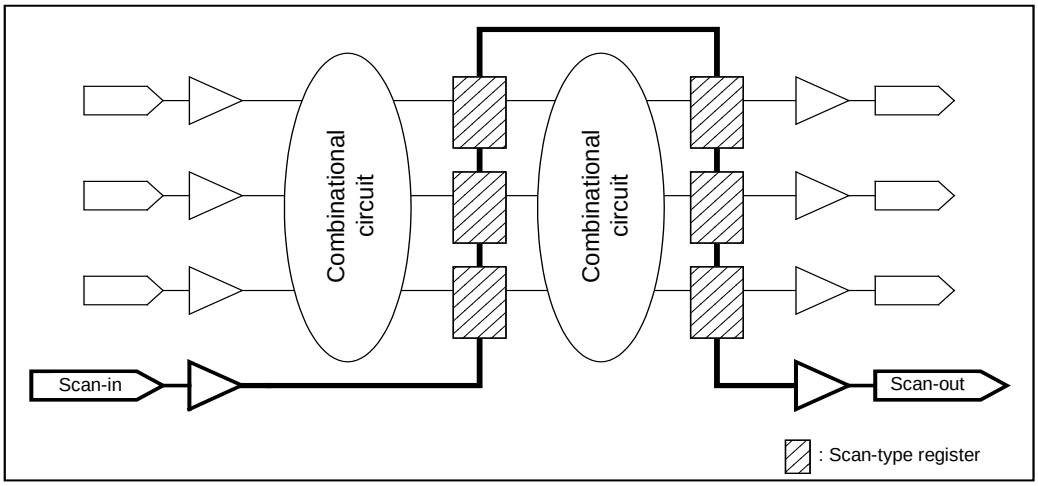


Figure 3-1 Example Scan Circuit

Note: The test patterns generated by ATPG are not intended for use in confirming specifications.
Transparent latches are not replaced with scan-type registers.

3.3 Boundary Scan (JTAG) Circuit Insertion

Please indicate in the development start order whether boundary scan (JTAG) circuits are to be inserted. Boundary scan (JTAG) circuits will be inserted by Epson.

When boundary scan (JTAG) circuits are inserted, boundary scan circuits complying with IEEE 1149.1 and their control circuits (TAP controllers) will be inserted around the logical circuits. A BDSL file containing information on these circuits will be provided at the same time.

The function patterns for the boundary scan circuits inserted will be prepared by Epson. There is no need for the customer to create boundary scan related patterns.

3.3.1 Instructions

The following boundary scan instructions are supported:

Table 3-1 List of Supported Instructions and Codes

Instruction	Code
SAMPLE/PRELOAD	0...10
BYPASS	1...11
EXTEST	0...00
CLAMP	Optional*1
HIGHZ	Optional*1
IDCODE	0...01

NOTE: *1: Epson will assign codes if they are not specified by the customer. Codes must be unique. The instruction bit width should be two to 32 bits. This will also be specified by Epson if not specified by the customer.

3.3.2 Gate Count Estimation

The increase in gate count due to boundary scan circuit insertion varies depending on factors such as supported instructions and instruction bit width. Use the following information to estimate the gate count:

Table 3-2 Gate Count Estimation (BC: Basic cell calculation)

Boundary scan block	Gate count
TAP controller + miscellaneous gates	Approx. 1,000 (BCs)
Input pin	When using normal cells: Approx. 30 (BCs/pin) When using dedicated monitoring cells: Approx. 15 (BCs/pin)
2-state output pin	Approx. 35 (BCs/pin)
3-state output pin	Approx. 65 (BCs/pin)
Bi-directional pin	Approx. 95 (BCs/pin)

3.3.3 Boundary Scan (JTAG) Circuit Insertion in Customer Design

Please observe the following design rules if JTAG circuits are inserted as part of the customer's design:

(1) Boundary scan circuits cannot coexist with AC/DC test circuits

Bundary scan circuits cannot coexist with test circuits recommended by Epson. If boundary scans are supported, the recommended AC/DC test circuits cannot be inserted.

Characters usable for external pin names:

External pin names are subject to the following constraints imposed by the BSDL format rules:

① Only alphanumeric characters (a to z, A to Z, and 0 to 9) and the underscore ("_") character can be used.

② External pin names are not case sensitive. (CLK and clk are considered identical character strings.)

③ External pin names must start with a letter of the alphabet. (0CLK, _CLK are prohibited.)

④ External pin names must not include consecutive underscores. (SYS__CLK is prohibited.)

⑤ External pin names should not end with an underscore. (CLK_ is prohibited.)

(2) Dedicated external pin preparation

Boundary scan circuits always require five dedicated external pins. Insert external pins according to the following rules:

① Clock (TCK)
Clock pin for the boundary scan circuit. Provide an input cell with the output port not connected to anywhere.

② Mode select (TMS)
Mode select pin for the boundary scan circuit. Provide an input cell with the output port not connected to anywhere. The input cell used here should have a pull-up resistor.

③ Data input (TDI)
Scan data input pin for the boundary scan circuit. Provide an input cell with the output port not connected to anywhere. The input cell used here should have a pull-up resistor.

④ Data output (TDO)
Scan data output pin for the boundary scan circuit. Use a 3-state output cell with the input port pulled down.

⑤ Reset (TRST)
Asynchronous reset pin for the boundary scan circuit. Provide an input cell with the output port not connected to anywhere. The input cell used here should have a pull-up resistor.

```
IBC U1 ( .PAD(TCK) );                          // IBC:     Normal input cell
IBCP1 U2 ( .PAD(TMS) );                        // IBCP1:   Input cell with pull-up resistor
IBCP1 U3 ( .PAD(TDI) );
IBCP1 U4 ( .PAD(TRST) );
TB1 U5 ( .PAD(TDO), .A(1'b0),.E(1'b0) );       // TB1:     3-state output cell
```

Figure 3-2 Example Dedicated Pin Description (Using Verilog)

(3) Hierarchical blocks

The hierarchical blocks of the netlist should have the following structure. Hierarchical blocks such as a TAP controller are added after boundary scans are inserted.

- Place the I/O cells in the top block.
- Place other logic elements in the sub block immediately below the top block, where possible.

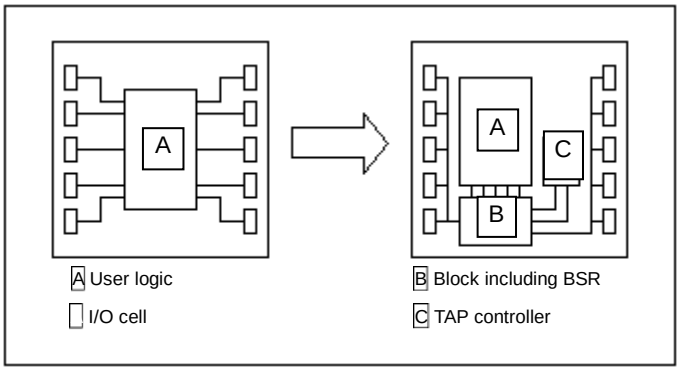


Figure 3-3 Hierarchical Block Structure Schematic

(4) I/O cell types

Boundary scan is not supported if the following I/O cells are used:

- I/O cell with test mode
- Gated input cell
- Open drain output cell

(5) External pins for analog signals

Boundary scan cells are not inserted for oscillator circuit input/output pins and external pins for analog signals.

(6) Package pin and pad constraints

Package pins must be connected individually to pads on the chips on a one-to-one basis.

A package pin cannot be connected to multiple pads on a chip (multi bonding). Multiple pads cannot be interconnected (multi pad).

3.4 RAM Test Circuit: Memory BIST (Built-in Self Test)

Epson provides a memory BIST (built-in self test) in the form of a self-diagnostic circuit used to test the built-in memory.

The memory BIST will be inserted by Epson into the RTL or gate-level netlists provided by the customer.

Chapter 4 Test Pattern Generation Precautions

This chapter describes precautions for generating test patterns.

4.1 Sign-off Simulation Test Pattern Generation

4.1.1 Test Pattern Format

Once results have been obtained in the RTL simulation, provide the ASIC primary input/output signal waveform in VCD (value change dump) format. Note that extended VCD formats such as Extended VCD cannot be used. If you use external bi-directional pins, also output the enable signal waveform. Note that test benches described in HDL cannot be used in the Epson sign-off simulation.

Epson will convert the VCD to Epson's proprietary APF (advanced press format) test pattern format to perform the simulation. Figure 4-1 illustrates the conversion from VCD to APF. Each waveform is converted to signal values sampled once every reference cycle. Figure 4-2 shows an APF sample.

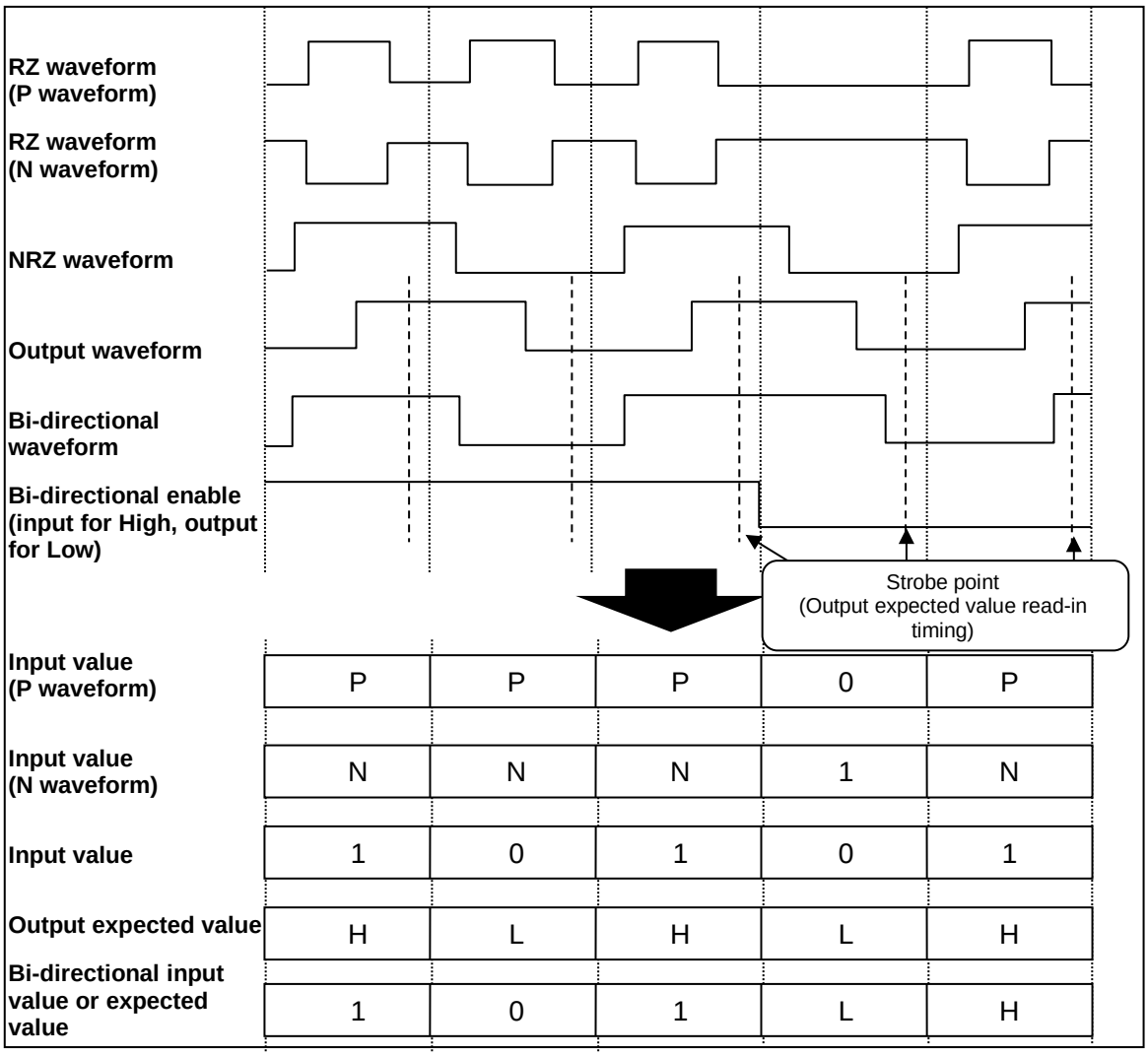


Figure 4-1 Schematic of Waveform Conversion to APF

```
# Create by Netlist Rule Check Utility at Fri Oct 6 11:42:55
$DESIGN     SAMPLE

$RATE           100000          <-- Rate (cycle) 100ns
$RESOLUTION     0.001ns
$STOROBE        85000           <-- Strobe point 85ns

#$HEX
#$ENDHEX

$IOCONT
inst01.ZO       E0      BID1
inst02.ZO       E0      BID2    <-- Internal node controlling bi-directional signal
$ENDIOCONT

$NODE
RST     I       10000           <-- Input pin with 10ns input delay
CLK     P       50000   90000   <-- Input pin with 50ns input delay, 40ns wide RZ waveform (P waveform)
XCLK    N       50000   90000   <-- Input pin with 50ns input delay, 40ns wide RZ waveform (N waveform)
INPUTB  IU      0
INPUTC  IU      0               <-- Input pin with 0ns input delay pull-up resistor
#
OUTA    O                       <-- Output pin
OUTB    O
#
BID1    B       0               <-- Bi-directional pin with 0ns input delay
BID2    B       30000
#
$ENDNODE

$PATTERN
#                   RCXIIOOBB
#                   SLCNNUUII
#                   TKLPPTTDD   <-- Input/output signal name (comment row)
#                     KUKAB12
#                      TT
#                      BC
#
#                   IPNIIOBB
#                                 <-- Event number (pattern cycle number)
#
  0                 1PN11XZ1L     <-- Signal value
  1                 1PN01XZ0L
  2                 1PN11XH1L
  3                 10101LHL1
  4                 1PN11LHH0

$ENDPATTERN
```

Note: Characters that can be used in signals

O: Input Low	1: Input High	P: P type RZ waveform input	N: N type RZ waveform input
L: Output Low	H: Output High	Z: Output high impedance	X: Unknown

Figure 4-2 APF Sample

4.1.2 Test Pattern Constraints

Epson performs a cycle-based simulation. Test patterns must comply with the constraints indicated below. STA analysis is required if you wish to rigorously check the input and output signal timing.

(1) Do not allow the clock cycle or pulse width to vary within the same VCD.

(2) Do not allow the skew between clocks or correlation between clock and input signal to vary within the same VCD. Ensure a constant input delay for each cycle.

(3) If clocks with different cycles exist within the same VCD, set the cycle for the fastest clock as the reference cycle time and specify cycles for other clocks as multiples of the reference cycle time.

(4) Set the P waveform clock to 0 input to stop it.

(5) Set the N waveform clock to 1 input to stop it.

(6) Unknown (X) and high impedance state (Z) cannot be input.

Figure 4-3 shows examples of input waveforms that cannot be used.

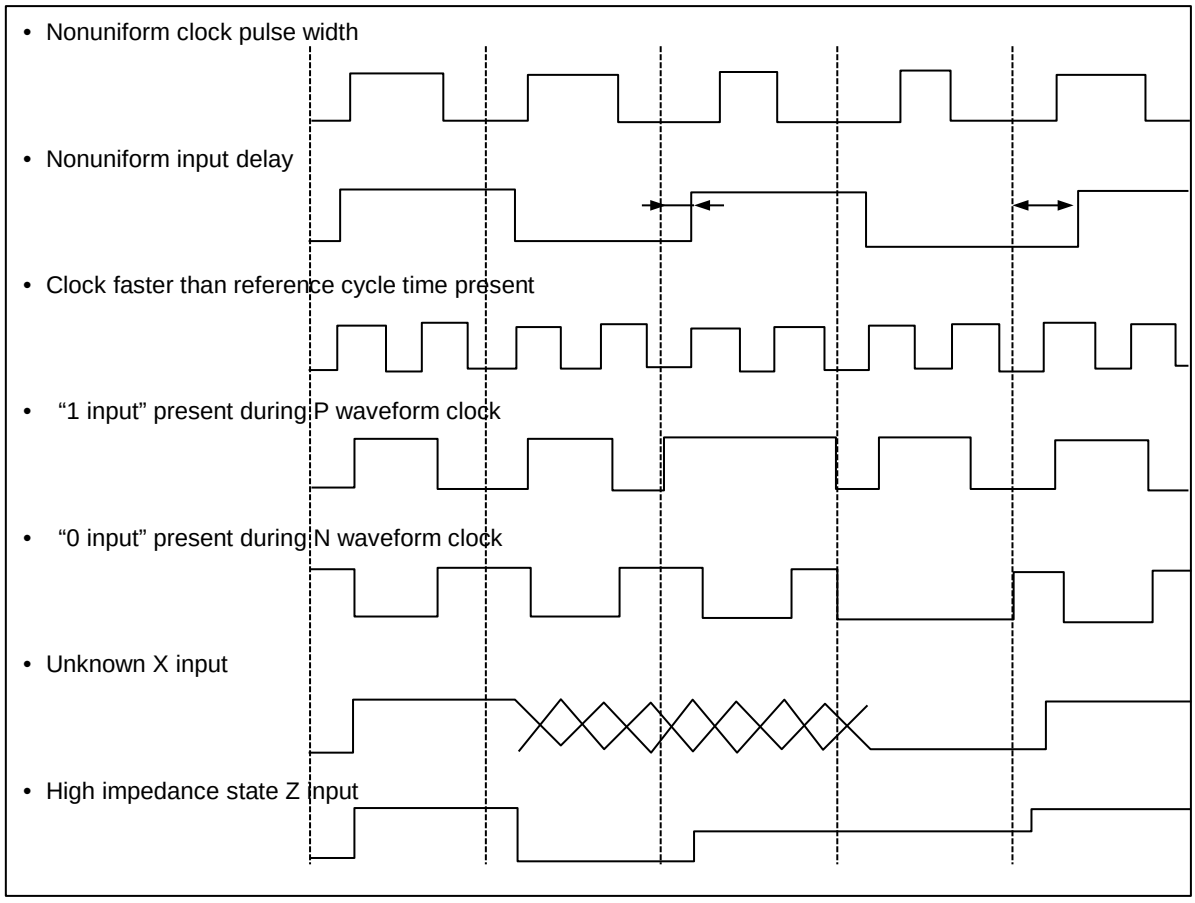


Figure 4-3 Invalid Input Waveform Examples

4.1.3 External Bi-directional Pin Enable Signal

If an external bi-directional pin is used, the waveform of the enable signal should be output accordingly. Here, make sure each external bi-directional pin is operated only by a single enable signal. If bi-directional enable signals within the RTL are configured with multiple signal logic (Figure 4-4), these must be replaced with a single signal (Figure 4-5).

```
inout data;
wire  data, cs, rd;
........
assign data = (cs & rd) ? outdata : 1'bz;
```

Figure 4-4 Bi-directional Enable Configured with Multiple Signal Logic

```
inout data;
wire  data, cs, rd, dataen;
........
assign dataen = cs & rd;
assign data = dataen ? outdata : 1'bz;
```

Figure 4-5 Replacing with Single Signal

4.2 Pre-shipment Test Pattern Generation

Epson will create pre-shipment test patterns based on test patterns received from the customer. Constraints apply due to IC tester capabilities, and changes will be made to ensure that test patterns for IC specification verification conform to the following constraints. Please note that the test patterns may need to be adjusted here in cases in which use of an IC tester is problematic—for example, if the test patterns are extremely long or if there are extremely large numbers of test patterns.

Please inform our sales representative if there are test patterns that do not require conversion for product pre-shipment testing or dedicated product pre-shipment test patterns.

4.2.1 Usable Input Waveforms

Test patterns are normally collections of 0 and 1, but delays may be added to input waveforms and pulses created when executing the simulation or when testing using an IC tester. The following two types of waveforms can be used when creating test patterns:

(1) NRZ (Non Return to Zero)

This is normally used for signals other than clocks. The signal can be varied once within a single rate to add a delay.

(2) RZ (Return to Zero)

This is used for clock and other signals. A positive or negative pulse can be generated within a single rate to efficiently create a clock signal. As with NRZ, a delay can be added.

4.2.2 Constraints on Test Patterns

Figure 4-6 shows the test rate, input delay, and pulse width to explain constraints that apply during test pattern generation.

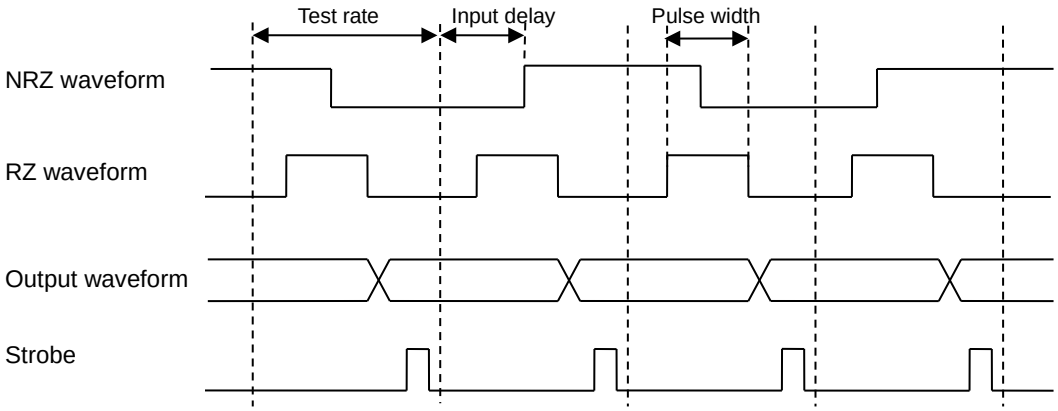


Figure 4-6 Test Pattern Timing

The constraints on test pattern generation are listed in (1) to (5) below.

(1) Constraints on test rates and number of events

Test rate:	100ns or more, in 1ns increments (Standard: 200ns)
Number of events per test pattern:	Up to 256,000 events
Number of test patterns:	Up to 30
Total number of test pattern events:	Up to 1 million events

(2) Input delay constraints

(a) Input delay range
Specify input delays within the range indicated below. For information on strobe point constraints, refer to "4.2.2 (5) Strobe constraints."
0ns ≤ Input delay < Strobe point

(b) Input delay phase difference
If a phase difference is added to an input delay, the difference should be at least 3ns.

(c) Input delay type
No more than eight different input delay types should occur within a single test pattern. A 0ns delay counts as one type here. Even if the delay value is the same, input delays are counted as different types if the waveform (RZ or NRZ) and pulse widths differ.

(3) Pulse width constraints

The RZ waveform pulse width must be set to at least 15ns.

(4) Input waveform format constraints

The input waveforms can use 0, 1, P, or N values. Here, P and N indicate the pulse input in RZ waveforms. P and N values cannot be specified other than as combinations of 0 and P or 1 and N for the same pin within a single test pattern.

For bi-directional pins, RZ waveforms can be input only when there is no output state within a single test pattern.

(5) Strobe constraints

(a) Only one strobe type can be defined for each test pattern.

(b) The strobe minimum value must be at least 30ns after all output signals have stopped changing due to the applied input signal for all events.

(c) The strobe maximum value must be smaller than the test rate minus 15ns.

(d) Strobes must be set in 1ns increments.

4.2.3 Creating AC/DC Test Patterns

For AC and DC testing, Epson will create AC and DC test patterns for the recommended Epson test circuits inserted on behalf of the customer.

Customers wishing to insert an AC or DC test circuit on their own should create test patterns, referring to "A3. AC/DC Test Patterns."

4.2.4 Notes on Handling High Impedance State

Epson prohibits the high impedance state of input pins during simulations because correct operation cannot be guaranteed.

I/O cells are available with pull-up or pull-down resistors as a measure against high impedance. However, propagation delay times for pull-up and pull-down resistors are not considered in the simulation for the reasons indicated below. Since this prevents accurate simulation of operations, the open state of bi-directional pins with pull-up or pull-down resistors in input mode is also prohibited.

<Reasons why the propagation delay of pull-up and pull-down resistors is not considered>

(1) Delay varies significantly depending on external load capacitance.

(2) Pull-up and pull-down resistors are intended only to avoid floating gates due to the high impedance state.

Before running the simulation, the test patterns are checked for the above issues using a tool. If “Z” is detected, indicating a high impedance state, the test pattern must be modified.

For the same reasons, a warning is also issued for “Z” with bi-directional pins with pull-up or pull-down resistors. Open drain bi-directional pins are also treated in the same way.

<Measures>

All “Z” occurrences for bi-directional pins are reported as errors in the test pattern check. (“Z” is excluded for 3-state and open drain output pins.)

To avoid these errors, a utility program is provided which replaces “Z” for bi-directional pins with pull-up resistors with “1” and “Z” for bi-directional pins with pull-down resistors with “0.”

If a bi-directional pin switches to input mode while “X” is output, “X” is propagated as an input signal during the simulation, whether or not the pin has a pull-up or pull-down resistor, and “?” is output as the simulation result. Correct the “?” and run the simulation again.

Table 4-1 Handling Bi-directional Pin Signals in Simulation

Input pattern	I/O mode	Simulation	Simulation result (output pattern)
“X”	Input mode	“X”	“?”
“1”, “H”	Input mode	“1”	“1”
“0”, “L”	Input mode	“0”	“0”

Chapter 5 Design Restrictions and Limitations

This chapter describes points to note regarding oscillator circuits, preventing contention with an external bus, and metastable countermeasures.

5.1 Oscillator Circuits

5.1.1 Oscillator Circuit Configuration

Two types of dedicated oscillator cells are provided for configuring oscillator circuits with the S1L5V000 Series: crystal oscillation and CR oscillation types.

The crystal oscillation type is further subdivided into the intermittent type (Figure 5-1) located in the IC internal cell area and the continuous type (Figure 5-2) located in the I/O cell area. When using the intermittent oscillation type as the continuous oscillation type, the E pin of the oscillator cell must be used as “H”.

CR oscillator circuits will be as shown in Figure 5-3.

The following are examples of oscillator circuit configurations:

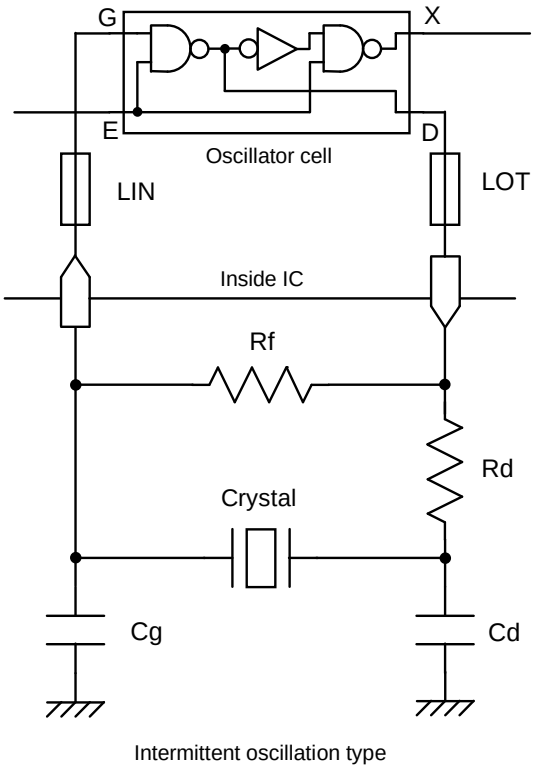


Figure 5-1 Crystal Oscillator Circuits (Located in Internal Cell Area)

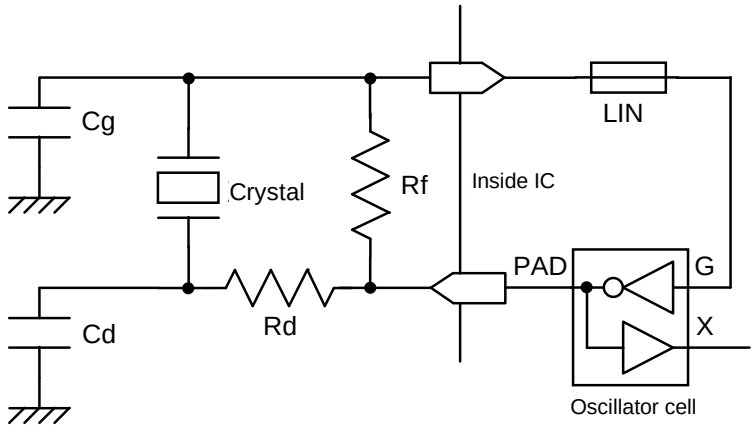


Figure 5-2 Crystal Oscillator Circuits (Located in I/O Cell Area)

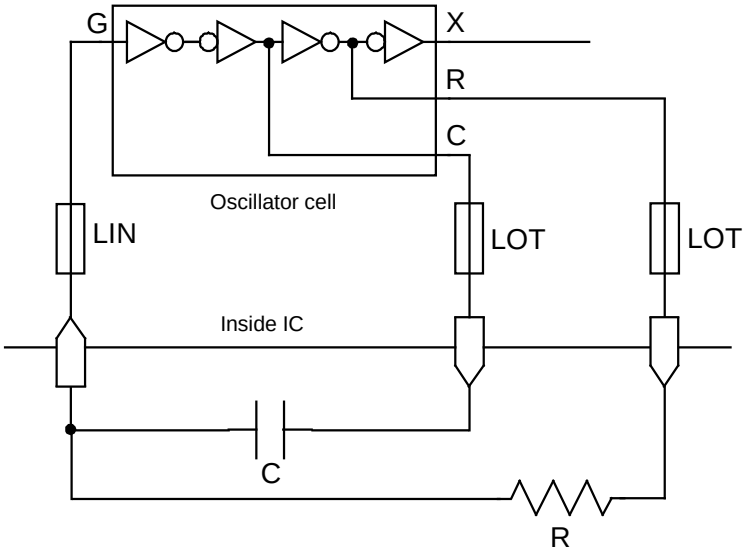


Figure 5-3 CR Oscillator Circuit

5.1.2 Notes When Using Oscillator Circuits

(1) Pinout

① Place the input and output pins of the oscillator circuit next to each other, between the power supply pins (V_{DD}, V_{SS}) on either side.

② Place the input and output pins of the oscillator circuit at a distance from other output pins, especially from those in phase or out of phase with the oscillation waveform. Place these output pins on the opposite side of the package.

③ Place the input and output pins of the oscillator circuit at a distance from input pins that operate at high speed, such as a clock.

④ Place the input and output pins of the oscillator circuit as close as possible to the center of one of the four package sides.

⑤ If multiple oscillator circuits are embedded, place the circuits at a distance from one another to prevent interference.

⑥ If using a BGA or other area array package, contact our sales representative regarding the pinout.

(2) Guide to selecting oscillator cells

Oscillation frequencies range from several tens of kilohertz to several tens of megahertz. For more information, contact our sales representative.

(3) Setting external resistance and capacitance

Oscillator circuit characteristics are dependent on the elements of the circuit (IC, crystal, Rf, Rd, Cg, Cd, and the board). Select the optimal characteristics by mounting the components on the actual board and thoroughly evaluating the values of external Rf, Rd, Cg, and Cd.

(4) Guarantee level

The oscillator circuit characteristics are dependent on the elements of the circuit (IC, crystal, Rf, Rd, Cg, Cd, and the board). Thus, Epson cannot guarantee the oscillation operation or characteristics. The customer should thoroughly evaluate and confirm oscillation characteristics using ES samples.

(5) Clock signal input to the IC internal circuit

Due to the difficulty of specifying the waveform of the clock signal to be generated (signal of the oscillator cell X) in advance, the logic simulator can accurately handle only the clock frequency. For example, the actual clock duty of the IC will differ from simulation results.

Therefore, avoid using circuits utilizing both rising and falling times of the generated clock signal. Doing otherwise may produce circuits with errors not matching simulation results. Use circuits utilizing only the rising or falling time of the generated clock signal.

5.1.3 RTL Description for Oscillator Cells

For information on the RTL description of oscillator cells, refer to "2.6 Oscillator Cell Description."

5.2 Internal Bus Configuration

The bus circuit consists of 3-state logic circuits. Operating the bus control signal sets one of the outputs connected to the bus circuit to active (other outputs are in the high impedance state). One propagation signal line is shared by allocating accessible time.

Note the following when building an internal bus circuit using internal 3-state buffers:

(1) Bus cells can be used only for bus circuits. (See Table 5-1 for bus cells.)

(2) When building a bus circuit, attach a bus latch cell BLT* to the bus.

(3) Of the bus cells connected to a bus, only one output can be set to active (0 or 1); the other bus cell outputs must be set to high impedance state (Z).*1

(4) The fan-out of the bus cell connected to a bus must be within fan-out constraints.*2

(5) Bus circuits tend to suffer increased propagation delays due to fan-out effects and are therefore not suitable for high-speed operations.*2

(6) Data held by the bus latch cell should be used only to prevent floating; do not use it as a logic signal.*3

(7) Generate test patterns to enable the bus to be initialized easily.*4

(8) Bus control signal switching is allowed only once per cycle.

NOTE: *1: If multiple bus cells connected to a bus become active simultaneously (either 0 or 1), the output voltage level will become unstable, and a flow-through current will continually flow from V_{DD} to GND. To avoid this, this constraint must be met.

*2: If the load on the internal bus is excessive, the rising and falling times of signals will be extended due to longer wiring and increased connections. This makes it more likely that differences will arise between delays in logic simulations and actual device delays.

*3: Data is held by the bus latch cell even when all bus cells connected to a bus are set to the high impedance state (Z). However, to avoid affecting operations, the latch function is limited. Do not use data output held in the latch cell as valid data.

*4: Build the circuit to enhance testability by adding a test pin to improve bus controllability.

Table 5-1 Bus Cell List

Cell type	Cell name
Bus latches	BLT1, BLT4
Bus driver	TSBX2, TSBX4, TSBPX2
Inverting bus driver	TSVX2, TSVX4, TSVPX2

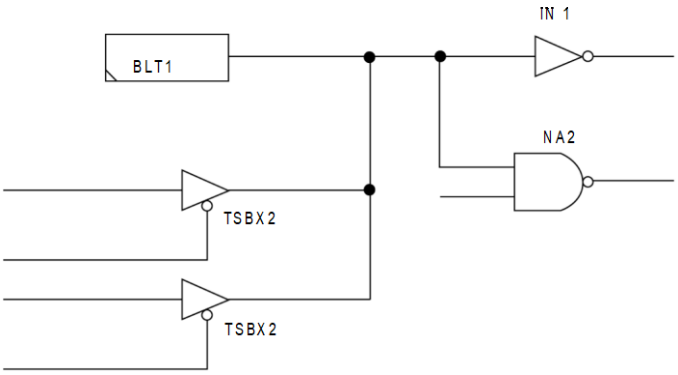


Figure 5-4 Bus Cell Circuit Example

5.3 Metastable

In the case of FF and latch cell input signals, if they violate timing rules, such as clock and data setup time, hold time, and release or removal time of clock set and reset, the FF and latch cell output signals may go neither high or low level. This unstable state of output signals is called “metastable.”

The metastable state ends after some time and output signals enter the defined state of either high or low level. However, the defined levels are not dependent on the data input level, and thus outputs are in unknown state.

When setup/hold and release/removal timing specifications are not met, take appropriate measures to prevent the metastable state from propagating to the whole circuit.

The metastable time is estimated using the following formula when setup/hold and release/removal time specifications are not met:

Metastable time = $T_{pd} \times 6$

Where T_{pd} is the delay time from the active edge of FF, latch cell clock, set, and reset signals to output change.

Logic simulation does not consider the delay of signals in the metastable state. Ensure that the design meets the timing specifications.

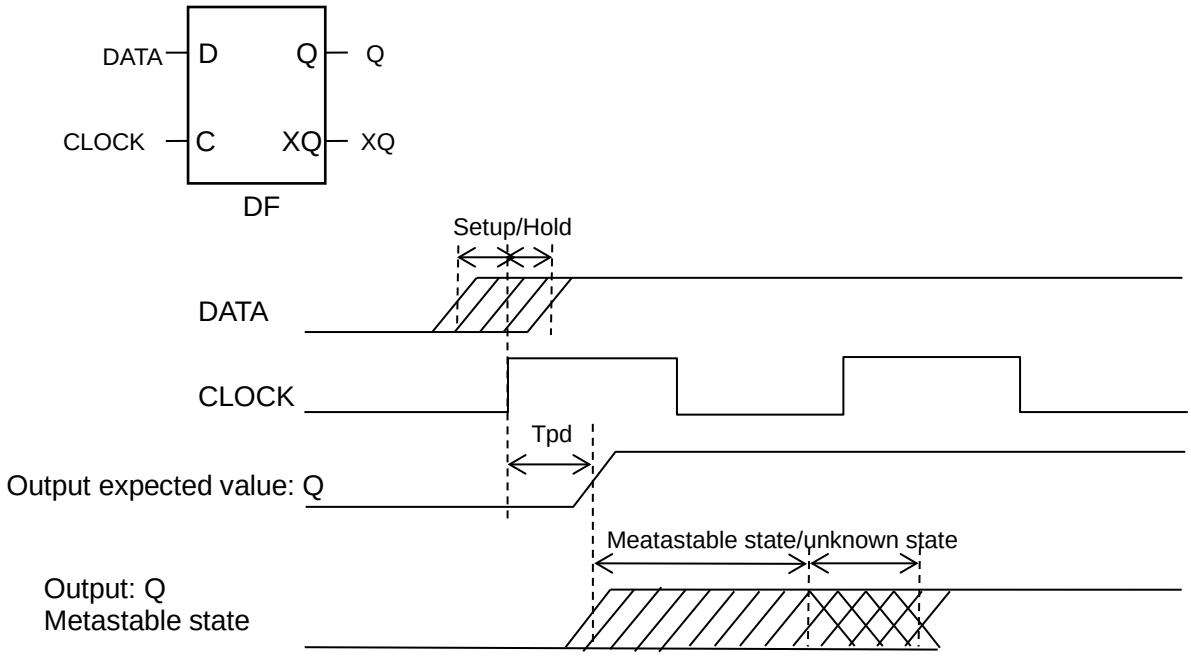


Figure 5-5 DF Metastable State

Chapter 6 Types of I/O Buffers and Notes on Use

6.1 I/O Buffer Types and Selection

I/O buffers are available for the S1L5V000 Series with different input interface levels, with or without Schmitt-trigger input, with or without pull-up or pull-down resistors, with different output drive capability, and with or without noise immunity. Select the required I/O buffers taking into account the following points.

For information on output drive capacity and pull-up and pull-down resistors, refer to Tables 1-5 and 1-6 in "1.3.3 Electrical Characteristics" and "A4. Input/Output Buffer Characteristics."

6.1.1 Selection of I/O buffers

A tool is provided for selecting I/O buffers. Refer to the following URL:

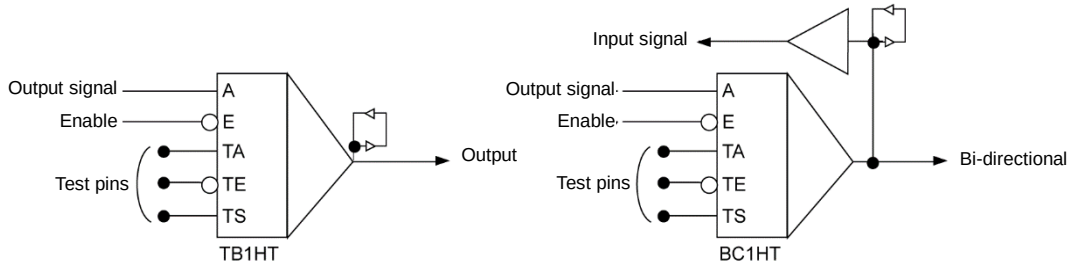
Design Guide supplementary information: S1L5V000 Series I/O Buffer List
<www.epson.jp/prod/semicon/products/asic/gatearray/s1l5v_io.htm>

6.1.2 I/O Buffers with Bus Hold Function

I/O buffers are available with a bus hold function that retains output pin data to prevent output pins or bi-directional pins from switching to the high impedance state.

Do not use the retained data output as valid data. The holding function of the bus hold circuit is restrained to avoid affecting normal operations. The data may vary easily if any other external data is supplied.

For information on output bus hold current, refer to Tables 1-5 and 1-6 in "1.3.3 Electrical Characteristics."



(a) Output buffer (b) Bi-directional buffer

Figure 6-1 Typical Bus Hold Circuit Symbols

6.2 I/O Buffer Configuration

The S1L5V000 Series can be used with a single power supply with a power supply voltage V_{DD} of 5.0V or 3.3V.

6.2.1 Input Buffers

Input buffers can be used at 5.0V or 3.3V.

Input buffers for V_{DD} = 5.0V and 3.3V are described below.
Input buffers are configured with input circuits only.

Table 6-1 shows the input buffer pull-up and pull-down resistance values.

Table 6-1 Pull-up/Pull-down Resistance Standards for Each Voltage

Pull-up/Pull-down Resistors	Resistance		Unit
	V_{DD} = 5.0V	V_{DD} = 3.3V	
Type 1	60	100	kΩ
Type 2	120	200	kΩ

Tables 6-2 and 6-3 list the input buffers for V_{DD} = 5.0V.

Table 6-2 Input Buffers (V_{DD} = 5.0V)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2*3
IBT	TTL	None
IBTP#	TTL	Pull-up resistor (60kΩ, 120kΩ)
IBTD#	TTL	Pull-down resistor (60kΩ, 120kΩ)
IBC	CMOS	None
IBCP#	CMOS	Pull-up resistor (60kΩ, 120kΩ)
IBCD#	CMOS	Pull-down resistor (60kΩ, 120kΩ)
IBS	TTL Schmitt	None
IBSP#	TTL Schmitt	Pull-up resistor (60kΩ, 120kΩ)
IBSD#	TTL Schmitt	Pull-down resistor (60kΩ, 120kΩ)
IBH	CMOS Schmitt	None
IBHP#	CMOS Schmitt	Pull-up resistor (60kΩ, 120kΩ)
IBHD#	CMOS Schmitt	Pull-down resistor (60kΩ, 120kΩ)

NOTE: *1: The # symbol corresponds to “1” for Type 1 resistance and “2” for Type 2 resistance.
*2: For more information on pull-down and pull-up resistances, refer to Table 1-5 and “A4.1.6.”
*3: For the input buffer characteristics graphs, refer to “A4.1.2.”

Table 6-3 Input Level Shifters (V_{DD} = 5.0V)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2*3
IDC	CMOS	None
IDCD#	CMOS	Pull-down resistor (60kΩ, 120kΩ)
IDH	CMOS Schmitt	None
IDHD#	CMOS Schmitt	Pull-down resistor (60kΩ, 120kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-down and pull-up resistances, refer to Table 1-5 and "A4.1.6."
*3: For the input buffer characteristics graphs, refer to "A4.1.2."

Tables 6-4 and 6-5 list the input buffers for V_{DD} = 3.3V.

Table 6-4 Input Buffers (V_{DD} = 3.3V)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2*3
IBC	LVTTL	None
IBCP#	LVTTL	Pull-up resistor (100kΩ, 200kΩ)
IBCD#	LVTTL	Pull-down resistor (100kΩ, 200kΩ)
IBH	LVTTL Schmitt	None
IBHP#	LVTTL Schmitt	Pull-up resistor (100kΩ, 200kΩ)
IBHD#	LVTTL Schmitt	Pull-down resistor (100kΩ, 200kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-down/pull-up resistance values, refer to Table 1-6.
*3: For the input buffer characteristics graphs, refer to "A4.2.2."

Table 6-5 Input Level Shifters (V_{DD} = 3.3V) (5V input also permitted)

Cell Name*1	Input Level	Pull-up/Pull-down Resistors*2*3
IDC	LVTTL	None
IDCD#	LVTTL	Pull-down resistor (100kΩ, 200kΩ)
IDH	LVTTL Schmitt	None
IDHD#	LVTTL Schmitt	Pull-down resistor (100kΩ, 200kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-down/pull-up resistance values, refer to Table 1-6.
*3: For the input buffer characteristics graphs, refer to "A4.2.2."

6.2.2 Output Buffers

Table 6-6 shows the I_{OL} and I_{OH} standards for output buffers.

Table 6-6 I_{OL}/I_{OH} Standards for Each Voltage

Output Current	I_{OL}*1/I_{OH}*2		Unit
	V_{DD} = 5.0V	V_{DD} = 3.3V	
Type S	0.1/-0.1	0.1/-0.1	mA
Type M	1/-1	1/-1	mA
Type 1	3/-3	2/-2	mA
Type 2	8/-8	6/-6	mA
Type 3	12/-12	12/-12	mA

NOTE: *1: V_{OL} = 0.4V
*2: $V_{OH} = V_{DD} - 0.4V$

Table 6-7 lists the output buffers for V_{DD} = 5.0V.
The "T" suffix in the cell name indicates an output buffer with a test circuit.

Table 6-7 Output Buffers (V_{DD} = 5.0V)

Function	I_{OL}/I_{OH}*1 *2	Cell Name
Normal output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	OBST OBMT OB1T OB2T OB3T
Normal output for high speed	3mA/-3mA 8mA/-8mA 12mA/-12mA	OB1CT OB2CT OB3AT
Normal output for low noise	12mA/-12mA	OB3BT
3-state output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	TBST TBMT TB1T TB2T TB3T
3-state output for high speed	3mA/-3mA 8mA/-8mA 12mA/-12mA	TB1CT TB2CT TB3AT
3-state output for low noise	12mA/-12mA	TB3BT
3-state output (with bus hold function)	1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	TBMHT TB1HT TB2HT TB3HT
3-state output for high speed (with bus hold function)	3mA/-3mA 8mA/-8mA 12mA/-12mA	TB1CHT TB2CHT TB3AHT
3-state output for low noise (with bus hold function)	12mA/-12mA	TB3BHT

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For more information on output currents, refer to "A4.1.3 Output Driver Characteristics."

Table 6-8 lists the output buffers for V_{DD} = 3.3V.
The "T" suffix in the cell name indicates an output buffer with a test circuit.

Table 6-8 Output Buffers (V_{DD} = 3.3V)

Function	I_{OL}/I_{OH}*1 *2	Cell Name
Normal output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 10mA/-10mA	OBST OBMT OB1T OB2T OB3T
Normal output for high speed	2mA/-2mA 6mA/-6mA 10mA/-10mA	OB1CT OB2CT OB3AT
Normal output for low noise	10mA/-10mA	OB3BT
3-state output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 10mA/-10mA	TBST TBMT TB1T TB2T TB3T
3-state output for high speed	2mA/-2mA 6mA/-6mA 10mA/-10mA	TB1CT TB2CT TB3AT
3-state output for low noise	10mA/-10mA	TB3BT
3-state output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 10mA/-10mA	TBMHT TB1HT TB2HT TB3HT
3-state output for high speed (with bus hold function)	2mA/-2mA 6mA/-6mA 10mA/-10mA	TB1CHT TB2CHT TB3AHT
3-state output for low noise (with bus hold function)	10mA/-10mA	TB3BHT

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to "A4.2.3 Output Driver Characteristics."

Table 6-9 shows the I_{OL} standards for N-channel open drain output buffers.

Table 6-9 N-Channel Open Drain Output Buffer I_{OL} Standards for Each Voltage

Output Current	I_{OL}*1		Unit
	V_{DD} = 5.0V	V_{DD} = 3.3V	
Type 1	3	2	mA
Type 2	8	6	mA
Type 3	12	10	mA

NOTE: V_{OL} = 0.4V

Tables 6-10 and 6-11 list the N-channel open drain output buffers.

Table 6-10 N-Channel Open Drain Output Buffers (V_{DD} = 5.0V)

Function	I_{OL}*1 *2	Cell Name
Normal output	3mA 8mA 12mA	OD1T OD2T OD3T
High speed output	3mA 8mA	OD1CT OD2CT

NOTE: *1: V_{OL} = 0.4V
*2: For more information on output currents, refer to "A4.1.3 Output Driver Characteristics."

Table 6-11 N-Channel Open Drain Output Buffers (V_{DD} = 3.3V)

Function	I_{OL}*1 *2	Cell Name
Normal output	2mA 6mA 10mA	OD1T OD2T OD3T
High speed output	2mA 6mA	OD1CT OD2CT

NOTE: *1: V_{OL} = 0.4V
*2: For more information on output currents, refer to "A4.2.3 Output Driver Characteristics."

6.2.3 Bi-directional Buffers

Tables 6-12-1, 6-12-2, and 6-13 list the bi-directional duffers for V_{DD} = 5.0V. Tables 6-14 and 6-15 list the bi-directional duffers for V_{DD} = 3.3V. The "T" suffix in the cell name indicates an output buffer with a test circuit.

Table 6-12-1 Bi-directional Buffers (1/2) (V_{DD} = 5.0V)

Input Level	Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
TTL	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	BTST BTMT BT1T BT2T BT3T	BTSD*T BTMD*T BT1D*T BT2D*T BT3D*T	BTSP*T BTMP*T BT1P*T BT2P*T BT3P*T
	Bi-directional output for high speed	12mA/-12mA	BT3AT	BT3AD*T	BT3AP*T
	Bi-directional output for low noise	12mA/-12mA	BT3BT	BT3BD*T	BT3BP*T
TTL Schmitt	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	BSST BSMT BS1T BS2T BS3T	BSSD*T BSMD*T BS1D*T BS2D*T BS3D*T	BSSP*T BSMP*T BS1P*T BS2P*T BS3P*T
	Bi-directional output for high speed	12mA/-12mA	BS3AT	BS3AD*T	BS3AP*T
	Bi-directional output for low noise	12mA/-12mA	BS3BT	BS3BD*T	BS3BP*T
CMOS	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	BCST BCMT BC1T BC2T BC3T	BCSD*T BCMD*T BC1D*T BC2D*T BC3D*T	BCSP*T BCMP*T BC1P*T BC2P*T BC3P*T
	Bi-directional output for high speed	3mA/-3mA 8mA/-8mA 12mA/-12mA	BC1CT BC2CT BC3AT	BC1CD*T BC2CD*T BC3AD*T	BC1CP*T BC2CP*T BC3AP*T
	Bi-directional output for low noise	12mA/-12mA	BC3BT	BC3BD*T	BC3BP*T
CMOS Schmitt	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	BHST BHMT BH1T BH2T BH3T	BHSD*T BHMD*T BH1D*T BH2D*T BH3D*T	BHSP*T BHMP*T BH1P*T BH2P*T BH3P*T
	Bi-directional output for high speed	3mA/-3mA 8mA/-8mA 12mA/-12mA	BH1CT BH2CT BH3AT	BH1CD*T BH2CD*T BH3AD*T	BH1CP*T BH2CP*T BH3AP*T
	Bi-directional output for low noise	12mA/-12mA	BH3BT	BH3BD*T	BH3BP*T

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to "A4.1.3 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 60kΩ or "2" for a resistance of 120kΩ.

Table 6-12-2 Bi-directional Buffers (2/2) (V_{DD} = 5.0V)

Input Level	Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
TTL	Bi-directional output (with bus hold function)	1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	BTMHT BT1HT BT2HT BT3HT	None	None
	Bi-directional output for high speed (with bus hold function)	12mA/-12mA	BT3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA	BT3BHT	None	None
TTL Schmitt	Bi-directional output (with bus hold function)	1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	BSMHT BS1HT BS2HT BS3HT	None	None
	Bi-directional output for high speed (with bus hold function)	12mA/-12mA	BS3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA	BS3BHT	None	None
CMOS	Bi-directional output (with bus hold function)	1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	BCMHT BC1HT BC2HT BC3HT	None	None
	Bi-directional output for high speed (with bus hold function)	3mA/-3mA 8mA/-8mA 12mA/-12mA	BC1CHT BC2CHT BC3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	12mA/-12mA	BC3BHT	None	None
CMOS Schmitt	Bi-directional output (with bus hold function)	1mA/-1mA 3mA/-3mA 8mA/-8mA 12mA/-12mA	BHMHT BH1HT BH2HT BH3HT	None	None
	Bi-directional output for high speed (with bus hold function)	3mA/-3mA 8mA/-8mA 12mA/-12mA	BH1CHT BH2CHT BH3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	Type 3 (12mA/-12mA)	BH3BHT	None	None

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to "A4.1.3 Output Driver Characteristics."

Table 6-13 N-Channel Open Drain Bi-directional Buffers (V_{DD} = 5.0V)

Input Level	Function	I_{OL} *1 *2	Cell Name
TTL	Bi-directional output	3mA 8mA 12mA	BDT1T BDT2T BDT3T
TTL Schmitt	Bi-directional output	3mA 8mA 12mA	BDS1T BDS2T BDS3T
CMOS	Bi-directional output	3mA 8mA 12mA	BDC1T BDC2T BDC3T
	Bi-directional output for high speed	3mA 8mA	BDC1CT BDC2CT
CMOS Schmitt	Bi-directional output	3mA 8mA 12mA	BDH1T BDH2T BDH3T
	Bi-directional output for high speed	3mA 8mA	BDH1CT BDH2CT

NOTE: *1: V_{OL} = 0.4V
*2: For output current characteristics, refer to "A4.1.3 Output Driver Characteristics-."

Table 6-14 Bi-directional Buffers (V_{DD} = 3.3V)

Input Level	Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
LVTTL	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 10mA/-10mA	BCST BCMT BC1T BC2T BC3T	BCSD*T BCMD*T BC1D*T BC2D*T BC3D*T	BCSP*T BCMP*T BC1P*T BC2P*T BC3P*T
	Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 10mA/-10mA	BC1CT BC2CT BC3AT	BC1CD*T BC2CD*T BC3AD*T	BC1CP*T BC2CP*T BC3AP*T
	Bi-directional output for low noise	10mA/-10mA	BC3BT	BC3BD*T	BC3BP*T
LVTTL Schmitt	Bi-directional output	0.1mA/-0.1mA 1mA/-1mA 2mA/-2mA 6mA/-6mA 10mA/-10mA	BHST BHMT BH1T BH2T BH3T	BHSD*T BHMD*T BH1D*T BH2D*T BH3D*T	BHSP*T BHMP*T BH1P*T BH2P*T BH3P*T
	Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 10mA/-10mA	BH1CT BH2CT BH3AT	BH1CD*T BH2CD*T BH3AD*T	BH1CP*T BH2CP*T BH3AP*T
	Bi-directional output for low noise	10mA/-10mA	BH3BT	BH3BD*T	BH3BP*T
LVTTL	Bi-directional output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 10mA/-10mA	BCMHT BC1HT BC2HT BC3HT	None	None
	Bi-directional output for high speed (with bus hold function)	2mA/-2mA 6mA/-6mA 10mA/-10mA	BC1CHT BC2CHT BC3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	10mA/-10mA	BC3BHT	None	None
LVTTL Schmitt	Bi-directional output (with bus hold function)	1mA/-1mA 2mA/-2mA 6mA/-6mA 10mA/-10mA	BHMHT BH1HT BH2HT BH3HT	None	None
	Bi-directional output for high speed (with bus hold function)	2mA/-2mA 6mA/-6mA 10mA/-10mA	BH1CHT BH2CHT BH3AHT	None	None
	Bi-directional output for low noise (with bus hold function)	10mA/-10mA	BH3BHT	None	None

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to "A4.2.3 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 100kΩ or "2" for a resistance of 200kΩ.

Table 6-15 N-Channel Open Drain Bi-directional Buffers (V_{DD} = 3.3V)

(5V can also be applied)

Input Level	Function	I_{OL} *1 *2	Cell Name
LVTTL	Bi-directional output	2mA 6mA 10mA	BDC1T BDC2T BDC3T
	Bi-directional output for high speed	2mA 6mA/-6mA	BDC1CT BDC2CT
LVTTL Schmitt	Bi-directional output	2mA 6mA 10mA	BDH1T BDH2T BDH3T
	Bi-directional output for high speed	2mA 6mA	BDH1CT BDH2CT

NOTE: *1: V_{OL} = 0.4V

*2: For output current characteristics, refer to "A4.2.3 Output Driver Characteristics."

6.3 Fail-Safe I/O Buffers

6.3.1 Outline

The S1L5V000 Series fail-safe I/O buffers for single power supply designs enable interfacing with signals that exceed the power supply voltage without the need for a dedicated interface power supply.

6.3.2 Features

(1) No constraints apply to cell count and placement, allowing placement to suit requirements.

(2) No large current flows other than the input leakage current in the fail-safe buffer, even when an input signal exceeding the power supply voltage is applied while the power supply is on.

(3) No large current flows other than the input leakage current in the fail-safe buffer, even when an external input signal is applied while the power is cut off.

(4) Two types of LVTTL/LVTTL Schmitt input levels (V_{DD} = 3.3V) are available.

6.3.3 Notes on Use

(1) If a signal exceeding the power supply voltage is input in High output mode, a relatively large current will flow in the same way as with regular I/O buffers. Care must be taken because this also happens when an external pull-up resistor greater than the power supply voltage exists.

(2) Note that the signal voltage that can be applied to a fail-safe buffer must not exceed the absolute maximum rating.

6.3.4 Cell Listing

(1) Fail-safe input buffers

Tables 6-16 to 6-18 list the fail-safe I/O buffers.
Input buffers allowing 5V input without pull-up will be input level shifters.

Table 6-16 Fail-Safe Input Buffers (V_{DD} = 3.3V) (5V input also permitted)

Cell Name*1	Input Level	Pull-up resistor*2 *3
IBBP#	LVTTL	Pull-up resistor (100kΩ, 200kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-up resistances, refer to Table 1-6.
*3: For the input buffer characteristics graphs, refer to "A4.2.2."

(2) Fail-safe output buffers

Table 6-17 Fail-Safe Output Buffers (V_{DD} = 3.3V)

Function	I_{OL}/I_{OH}*1 *2	Cell Name
3-state output	2mA/-2mA 6mA/-6mA	TBF1 TBF2
3-state output for high speed	2mA/-2mA 6mA/-6mA 12mA/-12mA	TBF1C TBF2C TBF3A

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to "A4.2.3 Output Driver Characteristics."

(3) Fail-safe bi-directional buffers

Table 6-18 Fail-Safe Bi-directional Buffers (V_{DD} = 3.3V)

Input Level	Function	I_{OL}/I_{OH}*1 *2	No Resistor	With Pull-down Resistor*3	With Pull-up Resistor*3
LVTTL	Bi-directional output	2mA/-2mA 6mA/-6mA	BB1 BB2	BB1D* BB2D*	BB1P* BB2P*
	Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 10mA/-10mA	BB1C BB2C BB3A	BB1CD* BB2CD* BB3AD*	BB1CP* BB2CP* BB3AP*
LVTTL Schmitt	Bi-directional output	2mA/-2mA 6mA/-6mA	BG1 BG2	BG1D* BG2D*	BG1P* BG2P*
	Bi-directional output for high speed	2mA/-2mA 6mA/-6mA 10mA/-10mA	BG1C BG2C BG3A	BG1CD* BG2CD* BG3AD*	BG1CP* BG2CP* BG3AP*

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to "A4.2.3 Output Driver Characteristics."
*3: The * symbol corresponds to "1" for a resistance of 100kΩ or "2" for a resistance of 200 kΩ.

(4) V_{DD} = 3.3V fail-safe configuration example

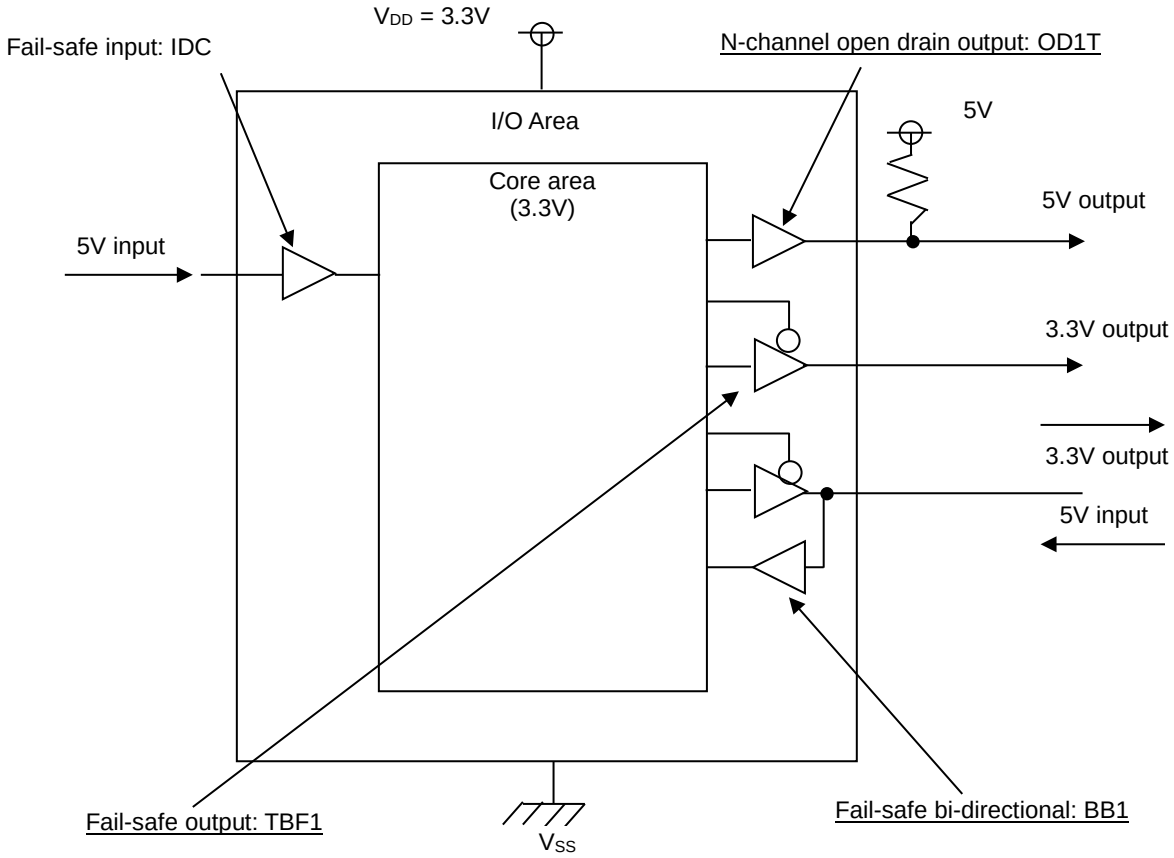


Figure 6-2 V_{DD} = 3.3V Fail-Safe Configuration Example

6.4 Gated I/O Buffers

6.4.1 Outline

The S1L5V000 Series gated I/O buffers allow the pin input to be set to floating state—i.e., to the high impedance state—without using a pull-up or pull-down resistor circuit. Buffers are available in two types: one that cuts off for a high level control signal and another that cuts off for a low level control signal. Select the type to suit the required level cut-off for the design.

6.4.2 Features

(1) No constraints on cell count and placement provide the designer with great flexibility to meet the customer's layout requirement.

(2) Possible to set the input to the high impedance state without using the pull-up or pull-down circuit.

(3) Two types of control signals are available: one for cutting off the current flow at the high level voltage and the other, at the low level voltage.

6.4.3 Notes on Use

(1) If the input changes to the high impedance state, use a control signal to cut off the input signal in advance. If the input changes from high impedance to 0 or 1, cancel the input signal cut-off after the change. A flow-through current may flow if this is not performed.

(2) Use a control signal to cut off the input signal before V_{DD} is cut off. Likewise, if V_{DD} turns on from cut-off, cancel the input signal cut-off once the power supply voltage has reached the rated level and the input signal has stabilized at 0 or 1.

6.4.4 Cell Listing

(1) Gated input buffers

Tables 6-19 list the gated input buffers.

Table 6-19 Gated Input Buffers

Cell Name*1	Input Type	Input Level	Pull-up/Pull-down Resistors	
			V_{DD} = 5.0V*2 *3	V_{DD} = 3.3V*4 *5
IBA	CMOS	AND Type	None	None
IBAP#	CMOS		Pull-up resistor (60kΩ, 120kΩ)	Pull-up resistor (100kΩ, 200kΩ)
IBAD#	CMOS		Pull-down resistor (60kΩ, 120kΩ)	Pull-down resistor (100kΩ, 200kΩ)
IBO	CMOS	OR Type	None	None
IBOP#	CMOS		Pull-up resistor (60kΩ, 120kΩ)	Pull-up resistor (100kΩ, 200kΩ)
IBOD#	CMOS		Pull-down resistor (60kΩ, 120kΩ)	Pull-down resistor (100kΩ, 200kΩ)

NOTE: *1: The # symbol corresponds to "1" for Type 1 resistance and "2" for Type 2 resistance.
*2: For more information on pull-up and pull-down resistances, refer to Table 1-5 and "A4.1.6."
*3: For the input buffer characteristics graphs, refer to "A4.1.2."
*4: For more information on pull-down/pull-up resistance values, refer to Table 1-6.
*5: For the input buffer characteristics graphs, refer to "A4.2.2."

(2) Gated bi-directional buffers

Table 6-20 Gated Bi-directional Buffers

Input Level		Function	I_{OL}/I_{OH}*1,		No Resistor	With Pull-down Resistor*4	With Pull-up Resistor*4
			V_{DD} = 5.0V*2	V_{DD} = 3.3V*3			
CMOS	AND Type	Bi-directional output	3mA/-3mA 8mA/-8mA 12mA/-12mA	2mA/-2mA 6mA/-6mA 10mA/-10mA	BA1T BA2T BA3T	BA1D*T BA2D*T BA3D*T	BA1P*T BA2P*T BA3P*T
		Bi-directional output for high speed	3mA/-3mA 8mA/-8mA 12mA/-12mA	2mA/-2mA 6mA/-6mA 10mA/-10mA	BA1CT BA2CT BA3AT	BA1CD*T BA2CD*T BA3AD*T	BA1CP*T BA2CP*T BA3AP*T
		Bi-directional output for low noise	12mA/-12mA	10mA/-10mA	BA3BT	BA3BD*T	BA3BP*T
	OR Type	Bi-directional output	3mA/-3mA 8mA/-8mA 12mA/-12mA	2mA/-2mA 6mA/-6mA 10mA/-10mA	BO1T BO2T BO3T	BO1D*T BO2D*T BO3D*T	BO1P*T BO2P*T BO3P*T
		Bi-directional output for high speed	3mA/-3mA 8mA/-8mA 12mA/-12mA	2mA/-2mA 6mA/-6mA 10mA/-10mA	BO1CT BO2CT BO3AT	BO1CD*T BO2CD*T BO3AD*T	BO1CP*T BO2CP*T BO3AP*T
		Bi-directional output for low noise	12mA/-12mA	10mA/-10mA	BO3BT	BO3BD*T	BO3BP*T

NOTE: *1: V_{OL} = 0.4V, V_{OH} = V_{DD} − 0.4V
*2: For output current characteristics, refer to "A4.1.3 Output Driver Characteristics."
*3: For output current characteristics, refer to "A4.2.3 Output Driver Characteristics."
*4: * is either 1 or 2.
With 1 corresponding to a resistance of 60kΩ and 2 corresponding to 120kΩ for V_{DD} = 5.0V
And 1 corresponding to a resistance of 100kΩ and 2 corresponding to 200kΩ for V_{DD} = 3.3V

Chapter 7 Notes on Pinout

This chapter discusses the points the designer needs to pay special attention when deciding package pinout and adding power supply pins to avoid malfunctions due to simultaneous switching of output buffers.

7.1 Estimating Power Supply Pin Count

The designer needs to estimate the power supply pin count according to the IC power consumption and output buffer count. Care must be taken especially for output buffers, as significant amount of transient current flows when they switch. The greater the output buffer drivability is, the larger transient current flows.

The following describes how to estimate the power supply pin count required for an IC in relation to the consumption current:

If the consumption current is I_{DD} [mA], the power supply pin count N_{IDD} is estimated as follows in relation to the consumption current:

$N_{IDD} \geq I_{DD} \div 50$ (pair): That is, up to 50mA can be supplied to one pair of V_{DD} and V_{SS} pins.

Notes: 1. At least one pair of power supply pins must be inserted in each side of the package. That is, at least 4 pairs of V_{DD} and V_{SS} pins are inserted for each package.
To obtain I_{DD}, calculate the power consumption using the formula discussed in Chapter 10, "10.1 Calculating Power Consumption," and then divide the power consumption by the operating voltage.
2. If the output buffer is connected to DC load and current steadily flows, power supply pins need to be added. For details, contact our sales representative.

7.2 Simultaneous Switching and Power Supply Addition

The maximum output drivability is 12mA (V_{DD} = 5.0V) for the S1L5V000 Series. Switching multiple output buffers simultaneously may generate large noise.

When a number of output buffers simultaneously switch, add power supplies referring to Tables 7-1 to 7-4 below to prevent noise-induced errors.

Table 7-1 V_{SS} Power Supply Addition for Output Buffer Simultaneous Switching (V_{DD} = 5.0V)

Output drivability (I_{OL})	Simultaneous switching count	Number of power supplies to add		
		CL ≤ 50pF	CL ≤ 100pF	CL ≤ 200pF
8mA	≤ 8	0	1	2
	≤ 16	1	2	4
	≤ 24	1	3	6
	≤ 32	2	4	8
12mA	≤ 8	1	2	3
	≤ 16	2	3	5
	≤ 24	2	5	7
	≤ 32	3	6	12

Table 7-2 V_{DD} Power Supply Addition for Output Buffer Simultaneous Switching (V_{DD} = 5.0V)

Output drivability (I_{OL})	Simultaneous switching count	Number of power supplies to add		
		CL ≤ 50pF	CL ≤ 100pF	CL ≤ 200pF
8mA	≤ 8	0	1	1
	≤ 16	1	1	3
	≤ 24	1	2	4
	≤ 32	1	3	5
12mA	≤ 8	1	2	3
	≤ 16	2	3	4
	≤ 24	3	4	5
	≤ 32	4	6	10

Table 7-3 V_{SS} Power Supply Addition for Output Buffer Simultaneous Switching (V_{DD} = 3.3V)

Output drivability (I_{OL})	Simultaneous switching count	Number of power supplies to add		
		CL ≤ 50pF	CL ≤ 100pF	CL ≤ 200pF
6mA	≤ 8	0	1	2
	≤ 16	1	2	3
	≤ 24	1	2	4
	≤ 32	2	3	5
12mA	≤ 8	1	2	2
	≤ 16	2	2	3
	≤ 24	2	3	5
	≤ 32	2	4	8

Table 7-4 V_{DD} Power Supply Addition for Output Buffer Simultaneous Switching (V_{DD} = 3.3V)

Output drivability (I_{OL})	Simultaneous switching count	Number of power supplies to add		
		CL ≤ 50pF	CL ≤ 100pF	CL ≤ 200pF
6mA	≤ 8	0	1	1
	≤ 16	1	1	2
	≤ 24	1	2	3
	≤ 32	1	2	3
12mA	≤ 8	1	2	2
	≤ 16	2	2	3
	≤ 24	2	3	3
	≤ 32	3	3	6

7.3 Notes on Pinout

After selecting the right device to suit a particular design, determine the package pinout. The power supply pin information and usable I/O pin count will then be estimated.

Please submit the pinout to Epson together with the development start order in the form of a “pinout table” (format unspecified) describing the pinout. Epson will then proceed with the placement and routing process based on the pinout table received from the customer.

7.3.1 Fixed Location Power Supply Pins

Depending on package combinations, some pins may be used only as power supply pins. For more information, please contact our sales representative.

7.3.2 Notes on Pinout

The pinout sometimes affects the IC logic functions and electrical characteristics. Also there may be constraints on pinout because of the IC packaging and the circuit or master configurations. The following describes points that require caution when determining the pinout, such as power supply current, input and output pin separation, critical signals, inputs with pull-up/pull-down resistors, simultaneous output switching, and high-current drivers.

(1) Power supply current (I_{DD}, I_{SS})

Power supply current (I_{DD}, I_{SS}) defines the allowable supply current flowing to the power supply pins when the device is active If the current exceeding this allowable value flows, the current density in the power lines within the IC becomes too high, and this may lower the IC reliability and even destroys the device. Also, the IC internal voltage either increases or decreases depending on the voltage generated by the current and wire resistance. This voltage change induces functional errors and inversely affects the DC or AC characteristics.

To prevent these problems, the current density and power line impedance need to be lowered. To achieve this, estimate the power consumption in the design phase, and ensure enough power supply pins to prevent excessive current from flowing through each power supply pin. For power supply pins, refer to “7.1 Estimating Power Supply Pin Count.” These power supply pins should not be placed close to each other, but should be scattered.

The total power supply pin count should include the power supply pins discussed above and additional power supply pins to reduce noise. For additional power supply pin count, see “7.2 Simultaneous Switching and Power Supply Addition.”

(2) Noise caused by output buffer operation

The following two types of noise occur due to the output buffer operation. To reduce these types of noise, one possible solution is to have as many power supplies as possible.

(a) Noise generated in power supply lines

Noise generated in power supply lines becomes an issue when a large number of output pins simultaneously switch; and it changes the IC input threshold level, which will end up with malfunctions. The noise in power supply lines occurs when large current flows through the power supply lines by the simultaneous switching of output buffers.

Inductance element affects power supply noise. The IC equivalent circuit is illustrated in Figure 7-1. In this circuit, when the output changes from high to low, the current flows into the IC from the output pin through the equivalent inductance L2, which is due to the IC package, etc. When this happens, the equivalent inductance L2 changes the voltage of IC internal V_{SS} power line. The voltage change in this V_{SS} power line is the noise that occurs to the power line. This noise is generated mainly by the equivalent inductance L2, and thus the quicker the power supply current changes, the larger noise occurs.

(b) Overshoot, undershoot, and ringing

Noise such as overshoot, undershoot and ringing, occurs due to the equivalent inductance of output pins. The L3 shown in Figure 7-1 is this equivalent inductance. Since inductance has the property to save energy, whether the output goes low or high, the saved energy makes the overshoot or undershoot proportional to the amount of flowing electric current and the rate of current change.

The most effective way to reduce overshoot or undershoot is use of output buffers with small drivability. As the load capacitance increases, overshoot or undershoot noise tends to become smaller. Therefore, care must be taken when using output buffers with high drivability.

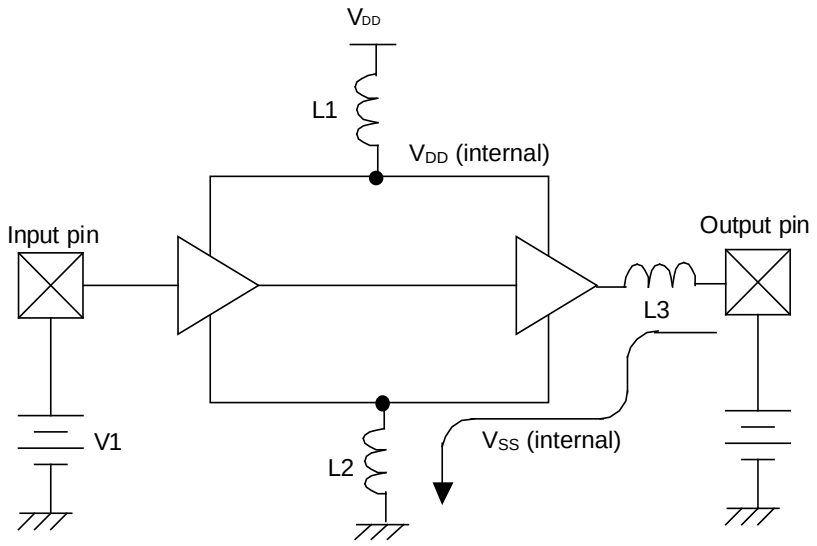


Figure 7-1 IC Equivalent Circuit

(3) Separating input and output pins

Separating the group of input pins from that of output pins is an important pinout technique to reduce noise effect.

To avoid the effect of noise generated from output pins, input pins and bi-directional pins in the input state must be positioned at a distance from output pins, where possible. Separate groups of input pins, output pins, and bi-directional pins from each other by corresponding power supply pins (V_{DD}, V_{SS}). (Figure 7-2)

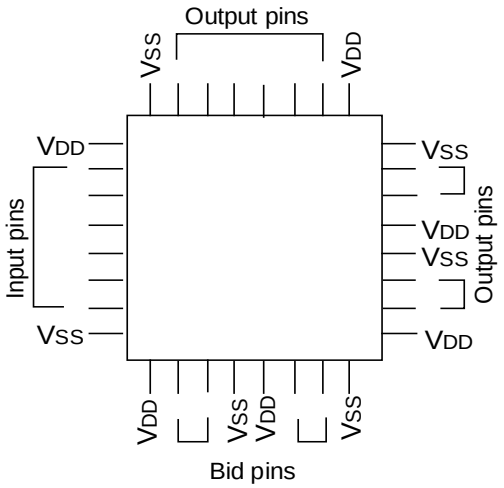


Figure 7-2 Example of Separating Input and Output Pins

(4) Critical signals

Pay attention to the following points for the pinout of critical signal pins such as clock input and high-speed output pins.

(a) Do not place clock and reset pins, that are vulnerable to noise, close to the output pins, but place them close to the power supply pins. (Figure 7-3)

(b) Place the high-speed input and output pins in the middle of the IC (package) side. (Figure 7-3)

(c) When the delay from an input pin to an output pin is hard to meet the customer's specification, place these input and output pins close to each other. (Figure 7-3)

(d) Place the oscillator circuit input and output pins (OSCIN, OSCOUNT) close to each other and enclose them by the power supply pins (V_{DD} and V_{SS}). Also, do not place the output pins synchronous to the oscillator circuit close to the output pins. (Figure 7-4)

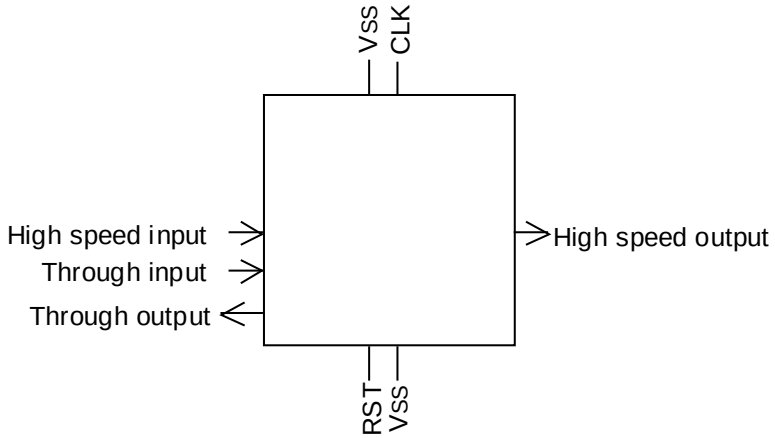


Figure 7-3 Critical Signal Pinout Example 1

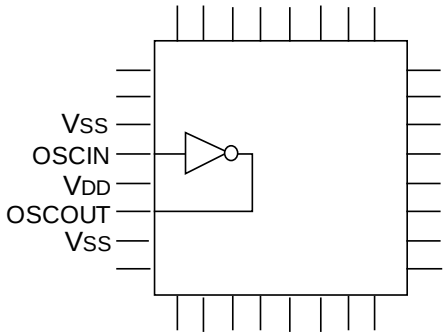


Figure 7-4 Critical Signal Pinout Example 2

(5) Inputs with pull-up/pull-down resistors

Pull-up/pull-down resistance is relatively large, from some tens of kilo-ohm to some hundreds of kilo-ohm, and dependent on the power supply voltage due to the resistor structure.

Note the following points when using these pins in the open state (e.g., for testing purposes). They are susceptible to power supply noise and may cause malfunctions.

(a) Place pull-up/pull-down resistor pins as far away from high-speed input pins (clock input pins, etc.) as possible.

Refer to Figure 7-5 Pull-up/Pull-down Resistor Input Pin Pinout Example 1.

(b) Place pull-up/pull-down resistor pins away from the output pins (especially from the high-current output pins).

Refer to Figure 7-6 Pull-up/Pull-down Resistor Input Pin Pinout Example 2.

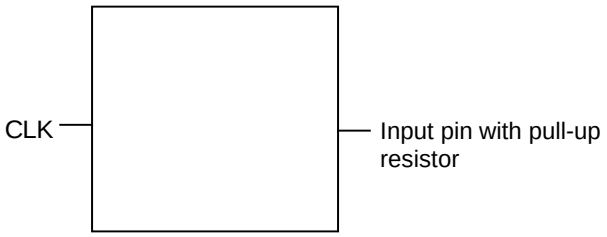


Figure 7-5 Pull-up/Pull-down Resistor Input Pin Pinout Example 1

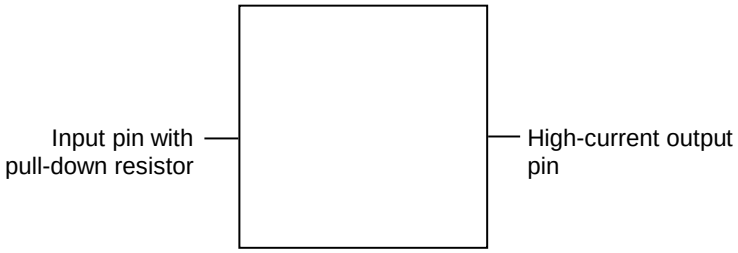


Figure 7-6 Pull-up/Pull-down Resistor Input Pin Pinout Example 2

In addition to the pinout notes, consider the following points in advance:

- Perform pull-up or pull-down process on the printed circuit board wherever possible.
- Select pins with the smallest possible resistance.

(6) Simultaneous output switching

Noise caused by simultaneous switching of output pins induces IC malfunctions. When switching many output pins simultaneously, add power supply pins to the group of output pins to avoid errors by noise. As for the number of required power supply pins and how to place additional power pins, refer to "7.2 Simultaneous Switching and Power Supply Addition." (Figure 7-7)

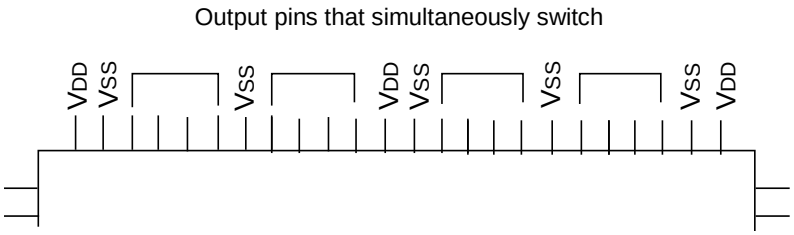


Figure 7-7 Example of Adding Power Supply Pins

Simultaneous signal switching and noise from output cells can be reduced by adding a delay cell to the input of the output cells in one group. (Figure 7-8)

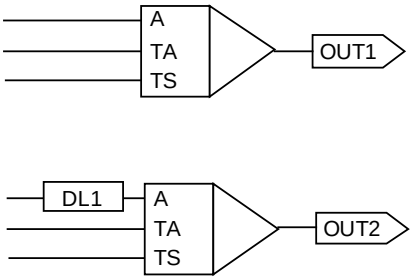


Figure 7-8 Example of Adding a Delay Cell

(7) High current drivers

When used with high current drivers (I_{OL} = 12mA), the pinout must comply with the following constraints:

(a) Constraint on power supply enhancement

Since high current drivers have high drivability, the noise that would occur when output buffers are active is also large, sometimes causing malfunctions to IC.

When using high current drivers, place the power supply pins close to the driver pins to secure power supply. (Figure 7-9)

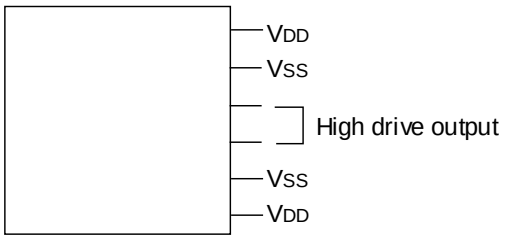


Figure 7-9 Example of Power Supply Enhancement

(8) Other notes

(a) NC pins (non-connection)

Do not connect anything to the NC pin.

7.3.3 Recommended Pinout

The pinout is important to have IC devices function correctly. The following is a pinout example that meets the constraints discussed above (Figure 7-10). Determine the pinout referring to the following example.

Table 7-5 describes the pins and pinout in the recommended pinout shown in Figure 7-10.

The input pins are placed at the upper and left sides of the package, the output pins that simultaneously switch are placed at the right side, and bi-directional and other output pins are placed at the lower side of the package.

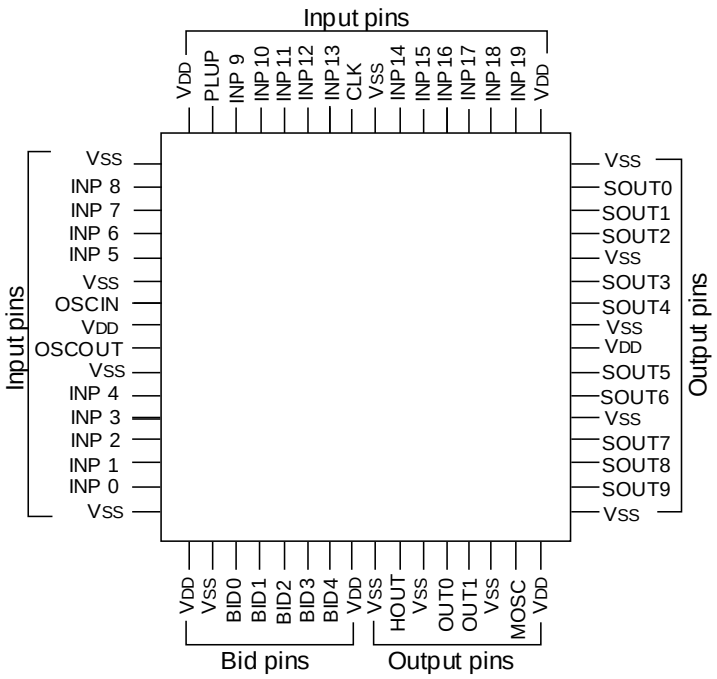


Figure 7-10 Recommended Pinout Example

Table 7-5 Description of Pinout Example

Place	Pin Name	Pin Name Description	Pinout Description
Upper Side	PLUP	Pull-up input pin	Place in the location where noise effect is small
	CLK	Clock iput pin	Place in the middle of the package side, and close to the power supply pin
Left Side	OSCIN	Oscillator pin	Place in the middle of the package side, and close to the power supply pin
	OSCOUT		Place in the middle of the package side, and close to the power supply pin
	INP0–19	Input pins	Separate from other pins by the power supply pin
Right Side	SOUT0–9	Simultaneous switching output pins	Separate from other pins by the power supply pin, and add power supply pins
Lower Side	BID0–4	Bi-directional pins	Seprate from other pins by the power supply pin
	MOSC	Oscillation monitor output pin	Place away from the oscillator pin, and close to the power supply pin
	HOUT	High-drivability output pin	Place close to the power supply pin
	OUT01	Output pin	Separate from other pins by the power supply pin
All Sides	V_{DD}	V_{DD} power supply pin	
	V_{SS}	V_{SS} (GND) power supply pin	

Chapter 8 RAM Specifications

The S1L5V000 Series supports asynchronous 1-port/2-port RAM and synchronous 1-port/2-port RAM.

8.1 Asynchronous 1-Port RAM

8.1.1 Features

(1) Asynchronous 1-port RAM

(2) Fully static operation

(3) One address port (shared read/write), one input data port, one output data port

(4) 16- to 256-word deep, configurable in 16-word increments
1- to 32-bit wide, configurable in 1-bit increments

(5) Maximum size: 8K bits/module

8.1.2 Word-Bit Configurations and RAM Cell Names

Table 8-1 shows RAM cell names corresponding to typical word-bit configurations. The RAM cells are named in accordance with the following rule, depending on the word-bit configuration.

1-port RAM: "V1N XXX YY" where "XXX" is the word depth (hexadecimal) and "YY" is the bit count (hexadecimal).

If asynchronous RAM for which the word-bit configuration exceeds the configurable range is required, configure using multiple asynchronous RAMs in combination.

Table 8-1 RAM Cell Naming for Asynchronous 1-port RAM Word-Bit Configuration Examples

Bit count / Word depth	4 bits	8 bits	16 bits	32 bits
32 words	V1N02004	V1N02008	V1N02010	V1N02020
64 words	V1N04004	V1N04008	V1N04010	V1N04020
128 words	V1N08004	V1N08008	V1N08010	V1N08020
256 words	V1N10004	V1N10008	V1N10010	V1N10020

8.1.3 RAM Size Estimation

Use the following formulas for estimating the BC count for X and Y directions:

X direction size: RX = 3 × Word/2 + 20
Y direction size: RY = 2 × Bit + 12
BC count: RAMBCS = RX × RY
Where Word is the word depth and Bit is the bit count

Table 8-2 Asynchronous 1-port RAM Configuration Examples and BC Counts

Bit count / Word depth	4 bits	8 bits	16 bits	32 bits
32 words	1,360 (68 × 20)	1,904 (68 × 28)	2,992 (68 × 44)	5,168 (68 × 76)
64 words	2,320 (116 × 20)	3,248 (116 × 28)	5,104 (116 × 44)	8,816 (116 × 76)
128 words	4,240 (212 × 20)	5,936 (212 × 28)	9,328 (212 × 44)	16,112 (212 × 76)
256 words	8,080 (404 × 20)	11,312 (404 × 28)	17,776 (404 × 44)	30,704 (404 × 76)

8.1.4 Function Descriptions

Table 8-3-1 Asynchronous 1-port RAM Signal Descriptions

Signal name	I/O	Function
CS	IN	Chip select signal, H: RAM active
RW	IN	Read/Write signal, H: Read, L: Write
A0, A1, ..., A (m-1)	IN	Read/Write address port, A0 : LSB
D0, D1, ..., D (n-1)	IN	Data input port, D0: LSB
Y0, Y1, ..., Y (n-1)	OUT	Data output port, Y0: LSB

Table 8-3-2 Asynchronous 1-port RAM Truth Table

CS	RW	A0, A1, ..., A (m-1)	Y0, Y1, ..., Y (n-1)	Mode
0	X	X	Unknown	Standby
1	0	Stable	Unknown	Write
1	1	Stable	Read data	Read

X: High or Low

(1) Data read

Set address with CS and RW held High to read data.

(2) Data write

There are two ways to write data:

① Set address with CS held High, and input Low-level pulse to RW.

② Set address with RW held Low, and input High-level pulse to CS.

In both cases, the RAM latches the data at the falling edge of the pulse.

(3) Standby state

When CS is Low, the 1-port RAM goes standby and only holds data. The current that flows through the RAM is only leakage current.

8.1.5 Timing Chart (Asynchronous 1-port RAM)

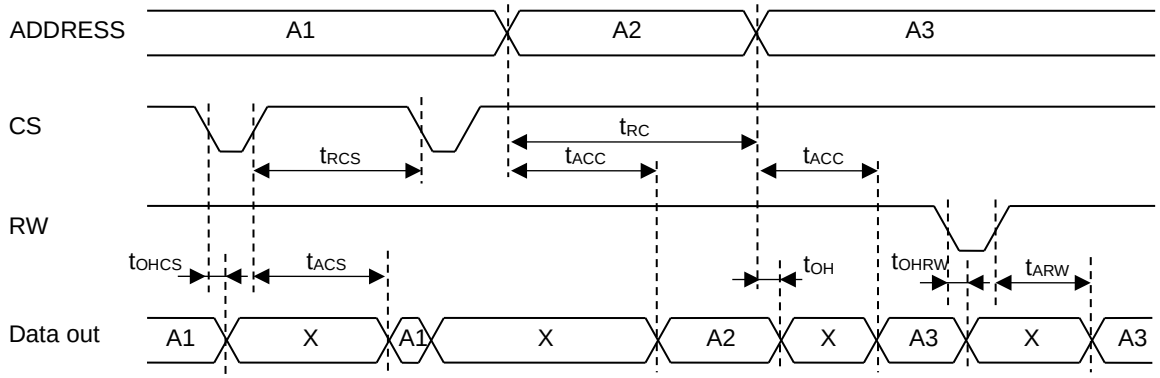


Figure 8-1 Read Cycle

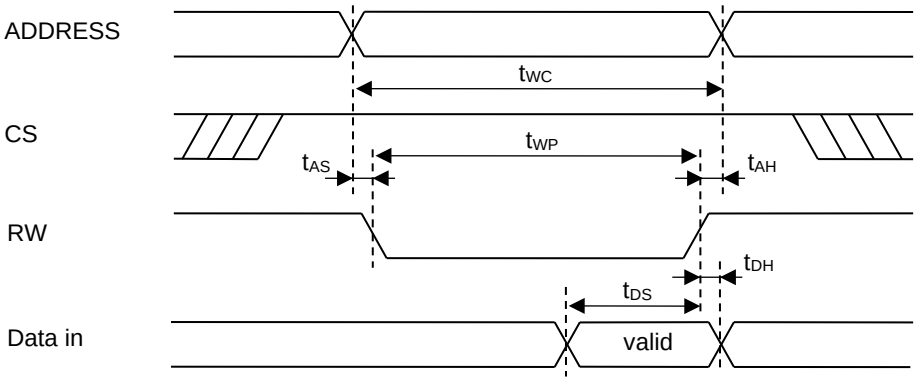


Figure 8-2 Write Cycle (RW Control)

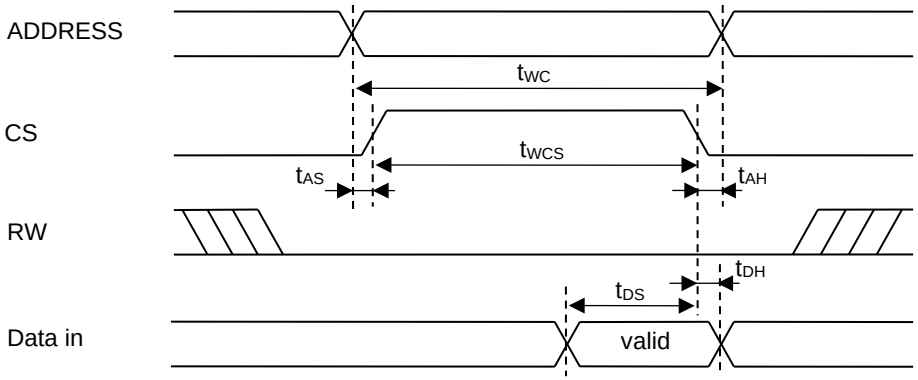


Figure 8-3 Write Cycle (CS Control)

8.2 Asynchronous 2-Port RAM

8.2.1 Features

(1) Asynchronous 2-port RAM

(2) Fully static operation

(3) Two address ports (separate read/write), one input data port, one output data port

(4) 16- to 256-word deep, configurable in 16-word increments
1- to 32-bit wide, configurable in 1-bit increments

(5) Maximum size: 8K bits/module

8.2.2 Word-Bit Configurations and RAM Cell Names

Table 8-4 shows RAM cell names corresponding to typical word-bit configurations. The RAM cells are named in accordance with the following rule, depending on the word-bit configuration.

2-port RAM: "V2N XXX YY" where "XXX" is the word depth (hexadecimal) and "YY" is the bit count (hexadecimal).

Table 8-4 RAM Cell Naming for Asynchronous 2-port RAM Word-Bit Configuration Examples

Bit count / Word depth	4 bits	8 bits	16 bits	32 bits
32 words	V2N02004	V2N02008	V2N02010	V2N020020
64 words	V2N04004	V2N04008	V2N04010	V2N04020
128 words	V2N08004	V2N08008	V2N08010	V2N08020
256 words	V2N10004	V2N10008	V2N10010	V2N10020

8.2.3 RAM Size Estimation

Use the following formulas for estimating the BC count for X and Y directions:

X direction size: RX = 3 × Word/2 + 20
Y direction size: RY = 2 × Bit + 15
BC count: RAMBCS = RX × RY
Where Word is the word depth and Bit is the bit count

Table 8-5 Asynchronous 2-port RAM Configuration Examples and BC Counts

Bit count / Word depth	4 bits	8 bits	16 bits	32 bits
32 words	1,564 (68 × 23)	2,108 (68 × 31)	3,196 (68 × 47)	5,372 (68 × 79)
64 words	2,668 (116 × 23)	3,596 (116 × 31)	5,452 (116 × 47)	9,164 (116 × 79)
128 words	4,876 (212 × 23)	6,572 (212 × 31)	9,964 (212 × 47)	16,748 (212 × 79)
256 words	9,292 (404 × 23)	12,524 (404 × 31)	18,988 (404 × 47)	31,916 (404 × 79)

8.2.4 Function Descriptions

Table 8-6-1 Asynchronous 2-port RAM Signal Descriptions

Signal name	I/O	Function
CS	IN	Chip select signal, H: RAM active
RD	IN	Read signal, H: Read enable
WR	IN	Write signal, H: Write enable
RA0, ... RA (m-1)	IN	Read address port, RA0: LSB
WA0, ... WA (m-1)	IN	Write address port, WA0: LSB
D0, D1, .. D (n-1)	IN	Data input port, D0: LSB
Y0, Y1, ... Y (n-1)	OUT	Data output port, Y0: LSB

Table 8-6-2 Asynchronous 2-port RAM Truth Table

CS	RD	WR	RA0, ..., RA（n-1）	WA0, ..., WA（m-1）	Y0, ..., Y（n-1）	Mode
0	X	X	X	X	Unknown	Standby
1	0	0	X	X	Unknown	Standby
1	0	1	X	Stable	Unknown	Write
1	1	0	Stable	X	Read data	Read
1	1	1	Stable	Stable	Read data	Read/Write

X: High or Low

(1) Data read

Set address with CS and RW held High to read data.

(2) Data write

There are two ways to write data:

① Set address with CS held High, and input High-level pulse to WR.

② Set address with WR held High, and input High-level pulse to CS.

(3) Data read and write

Simultaneous reading and writing is possible using read and write addresses. However, simultaneous read and write access to the same address is prohibited. As described in "8.3 Asynchronous RAM Delay Parameters," the read cycle access time is applicable to data for which the write operation has finished.

(4) Standby state

In the following two conditions, 2-port RAM will switch to standby and hold data only. The only consumption current that flows through the RAM is leakage current.

① When CS is Low

② When CS is High, RD is Low, and WR is Low

8.2.5 Timing Charts (Asynchronous 2-port RAM)

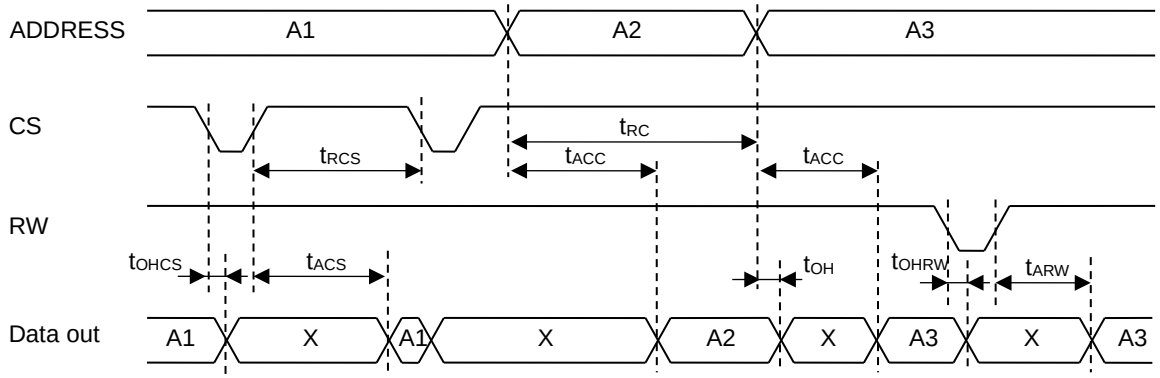


Figure 8-4 Read Cycle

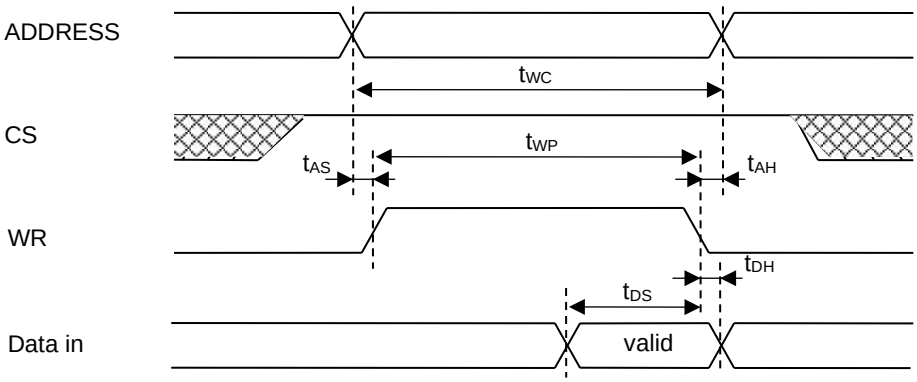


Figure 8-5 Write Cycle (WR Control)

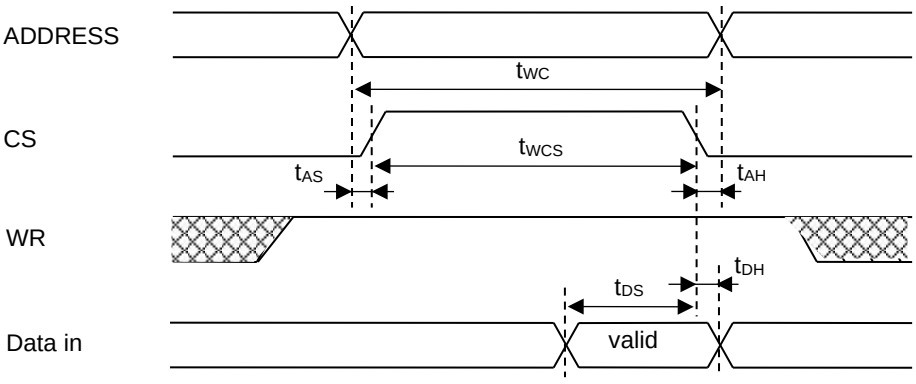


Figure 8-6 Write Cycle (CS Control)

8.3 Asynchronous RAM Delay Parameters

8.3.1 5.0V Specifications (V_{DD} = 4.5 to 5.5V, Ta = -40 to 110°C)

Table 8-7-1 Asynchronous 1-port/2-port RAM Read Cycle (1/2)

Parameter	Symbol	64word x 16bit V1N/V2N04010		64word x 32bit V1N/V2N04020		128word x 16bit V1N/V2N08010		128word x 32bit V1N/V2N08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	7.5	—	8.2	—	9.3	—	9.9	—	ns
Address access time	t_{ACC}	—	7.5	—	8.2	—	9.3	—	9.9	
CS access time	t_{ACS}	—	7.5	—	8.2	—	9.3	—	9.9	
RW access time	t_{ARW}	—	7.5	—	8.2	—	9.3	—	9.9	
CS active time	t_{RCS}	7.5	—	8.2	—	9.3	—	9.9	—	
Output hold time after address change	t_{OH}	0.1	—	0.2	—	0.1	—	0.2	—	
Output hold time after CS is disabled	t_{OHCS}	0.1	—	0.2	—	0.1	—	0.2	—	
Output hold time after RW is disabled	t_{OHRW}	0.1	—	0.2	—	0.1	—	0.2	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-7-1 Asynchronous 1-port/2-port RAM Read Cycle (2/2)

Parameter	Symbol	192word x 16bit V1N/V2N0C010		192word x 32bit V1N/V2N0C020		256word x 16bit V1N/V2N10010		256word x 32bit V1N/V2N10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	11.0	—	11.6	—	12.8	—	13.2	—	ns
Address access time	t_{ACC}	—	11.0	—	11.6	—	12.8	—	13.2	
CS access time	t_{ACS}	—	11.0	—	11.6	—	12.8	—	13.2	
RW access time	t_{ARW}	—	11.0	—	11.6	—	12.8	—	13.2	
CS active time	t_{RCS}	11.0	—	11.6	—	12.8	—	13.2	—	
Output hold time after address change	t_{OH}	0.1	—	0.2	—	0.1	—	0.2	—	
Output hold time after CS is disabled	t_{OHCS}	0.1	—	0.2	—	0.1	—	0.2	—	
Output hold time after RW is disabled	t_{OHRW}	0.1	—	0.2	—	0.1	—	0.2	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-7-2 Asynchronous 1-port/2-port RAM Write Cycle (1)

Parameter	Symbol	64word x 16bit V1N/V2N04010		64word x 32bit V1N/V2N04020		128word x 16bit V1N/V2N08010		128word x 32bit V1N/V2N08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	4.9	—	6.3	—	5.1	—	6.5	—	ns
Write pulse width	t_{WP}	2.3	—	3.7	—	2.3	—	3.7	—	
CS active time	t_{WCS}	2.3	—	3.7	—	2.3	—	3.7	—	
Address setup time	t_{AS}	0.9	—	0.9	—	1.1	—	1.1	—	
Address hold time	T_{AH}	1.7	—	1.7	—	1.7	—	1.7	—	
Data setup time	t_{DS}	0.0	—	0.0	—	0.0	—	0.0	—	
Data hold time	t_{DH}	2.7	—	3.9	—	2.9	—	3.9	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-7-2 Asynchronous 1-port/2-port RAM Write Cycle (2)

Parameter	Symbol	192word x 16bit V1N/V2N0C010		192word x 32bit V1N/V2N0C020		256word x 16bit V1N/V2N10010		256word x 32bit V1N/V2N10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	5.3	—	6.7	—	5.7	—	7.1	—	ns
Write pulse width	t_{WP}	2.5	—	3.9	—	2.7	—	4.1	—	
CS active time	t_{WCS}	2.5	—	3.9	—	2.7	—	4.1	—	
Address setup time	t_{AS}	1.1	—	1.1	—	1.3	—	1.3	—	
Address hold time	T_{AH}	1.7	—	1.7	—	1.7	—	1.7	—	
Data setup time	t_{DS}	0.0	—	0.0	—	0.0	—	0.0	—	
Data hold time	t_{DH}	2.9	—	4.1	—	3.1	—	4.1	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

8.3.2 3.3V Specifications (V_{DD} = 3.0 to 3.6V, Ta = -40 to 110°C)

Table 8-8-1 Asynchronous 1-port/2-port RAM Read Cycle (1/2)

Parameter	Symbol	64word x 16bit V1N/V2N04010		64word x 32bit V1N/V2N04020		128word x 16bit V1/V2N08010		128word x 32bit V1N/V2N08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	14.3	—	15.9	—	17.8	—	19.2	—	ns
Address access time	t_{ACC}	—	14.3	—	15.9	—	17.8	—	19.2	
CS access time	t_{ACS}	—	14.3	—	15.9	—	17.8	—	19.2	
RW access time	t_{ARW}	—	14.3	—	15.9	—	17.8	—	19.2	
CS active time	t_{RCS}	14.3	—	15.9	—	17.8	—	19.2	—	
Output hold time after address change	t_{OH}	0.2	—	0.3	—	0.2	—	0.3	—	
Output hold time after CS is disabled	t_{OHCS}	0.2	—	0.3	—	0.2	—	0.3	—	
Output hold time after RW is disabled	t_{OHRW}	0.2	—	0.3	—	0.2	—	0.3	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-8-1 Asynchronous 1-port/2-port RAM Read Cycle (2/2)

Parameter	Symbol	192word x 16bit V1N/V2N0C010		192word x 32bit V1N/V2N0C020		256word x 16bit V1N/V2N10010		256word x 32bit V1N/V2N10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	21.4	—	22.5	—	24.9	—	25.8	—	ns
Address access time	t_{ACC}	—	21.4	—	22.5	—	24.9	—	25.8	
CS access time	t_{ACS}	—	21.4	—	22.5	—	24.9	—	25.8	
RW access time	t_{ARW}	—	21.4	—	22.5	—	24.9	—	25.8	
CS active time	t_{RCS}	21.4	—	22.5	—	24.9	—	25.8	—	
Output hold time after address change	t_{OH}	0.2	—	0.3	—	0.2	—	0.3	—	
Output hold time after CS is disabled	t_{OHCS}	0.2	—	0.3	—	0.2	—	0.3	—	
Output hold time after RW is disabled	t_{OHRW}	0.2	—	0.3	—	0.2	—	0.3	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-8-2 Asynchronous 1-port/2-port RAM Write Cycle (1/2)

Parameter	Symbol	64word x 16bit V1N/V2N04010		64word x 32bit V1N/V2N04020		128word x 16bit V1N/V2N08010		128word x 32bit V1N/V2N08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	9.7	—	12.5	—	10.1	—	12.9	—	ns
Write pulse width	t_{WP}	4.5	—	7.3	—	4.5	—	7.3	—	
CS active time	t_{WCS}	4.5	—	7.3	—	4.5	—	7.3	—	
Address setup time	t_{AS}	1.8	—	1.8	—	2.2	—	2.2	—	
Address hold time	T_{AH}	3.4	—	3.4	—	3.4	—	3.4	—	
Data setup time	t_{DS}	0.0	—	0.0	—	0.0	—	0.0	—	
Data hold time	t_{DH}	5.3	—	7.7	—	5.7	—	7.7	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-8-2 Asynchronous 1-port/2-port RAM Write Cycle (2/2)

Parameter	Symbol	192word x 16bit V1N/V2N0C010		192word x 32bit V1N/V2N0C020		256word x 16bit V1N/V2N10010		256word x 32bit V1N/V2N10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	10.5	—	13.3	—	11.3	—	14.0	—	ns
Write pulse width	t_{WP}	4.9	—	7.7	—	5.3	—	8.0	—	
CS active time	t_{WCS}	4.9	—	7.7	—	5.3	—	8.0	—	
Address setup time	t_{AS}	2.2	—	2.2	—	2.6	—	2.6	—	
Address hold time	T_{AH}	3.4	—	3.4	—	3.4	—	3.4	—	
Data setup time	t_{DS}	0.0	—	0.0	—	0.0	—	0.0	—	
Data hold time	t_{DH}	5.7	—	8.0	—	6.1	—	8.0	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

8.4 Synchronous 1-port RAM

In addition to the clock asynchronous RAM described in section 8.1, clock synchronous RAM is also available for the S1L5V000 Series. This includes latch circuits for chip selection, write enable, address, and data input areas, allowing high-speed operation synchronized with the clock.

8.4.1 Features

(1) Clock synchronized 1-port RAM

(2) Latch circuits for chip select, write enable, address, and data input areas, allowing high-speed operation synchronized with the clock

(3) Separate data input and output ports

(4) 16- to 256-word deep, configurable in 4-word increments
1- to 32-bit wide, configurable in 1-bit increments

(5) Maximum size: 8K bits/module

8.4.2 Word-Bit Configurations and RAM Cell Names

Table 8-9 shows RAM cell names corresponding to typical word-bit configurations. The RAM cells are named in accordance with the following rule, depending on the word-bit configuration.

1-port RAM: "V1S XXX YY" where "XXX" is the word depth (hexadecimal) and "YY" is the bit count (hexadecimal).

If synchronous RAM for which the word-bit configuration exceeds the configurable range is required, configure using multiple synchronous RAMs in combination.

Table 8-9 Synchronous 1-port RAM Cell Names According to Word-Bit Configuration

Bit count / Word depth	4 bits	8 bits	16 bits	32 bits
32 words	V1S02004	V1S02008	V1S02010	V1S02020
64 words	V1S04004	V1S04008	V1S04010	V1S04020
128 words	V1S08004	V1S08008	V1S08010	V1S08020
256 words	V1S10004	V1S10008	V1S10010	V1S10020

8.4.3 RAM Size Estimation

Use the following formulas for estimating the BC count for X and Y directions:

X direction size: $RX = (\text{Word depth} \div 4) \times 7 + 35$
Y direction size: $RY = \text{Bit count} \times 2 + 9 + \alpha$
BC count: $RAMBCS = RX \times RY$
Where α is 3 when $16 \leq$ word depth ≤ 32 and 4 when $36 \leq$ word depth ≤ 256

Table 8-10 Synchronous 1-port RAM Configuration Examples and BC Count

Bit count / Word depth	4 bits	8 bits	16 bits	32 bits
32 words	1,820 (91 × 20)	2,548 (91 × 28)	4,004 (91 × 44)	6,916 (91 × 76)
64 words	3,087 (147 × 21)	4,263 (147 × 29)	6,615 (147 × 45)	11,319 (147 × 77)
128 words	5,439 (259 × 21)	7,511 (259 × 29)	11,655 (259 × 45)	19,943 (259 × 77)
256 words	10,143 (483 × 21)	14,007 (483 × 29)	21,735 (483 × 45)	37,191 (483 × 77)

8.4.4 Function Descriptions

(1) I/O signals

Table 8-11 Synchronous 1-port RAM Signal Descriptions

I/O signal		Function description
Symbol	Name	
CK	Clock input	Latches chip select (XCS), write enable (XWE), address input (A0 to An), and data input (D0 to Dn) at the clock input (CK) rising edge (L → H) and retains inside RAM.
XCS	Chip select	Latched at the clock input (CK) rising edge. Operation starts when the latched value is L.
XWE	Write enable	Latched at the clock input (CK) rising edge. Writing is performed when the latched value is L and reading is performed when the value is H.
A0 to An	Address input	Latched at the clock input (CK) rising edge.
D0 to Dn	Data input	Latched at the clock input (CK) rising edge. Writing to the memory cell is performed when write enable (XWE) is L.
Y0 to Yn	Data output	Data is output from the memory cell once the access time has elapsed after the clock input (CK) rising edge during reading. During writing, data written is output to this pin synchronized with CK. Note that the data read first will not be retained during writing.

(2) Operation description

Writing enables (sets to L) chip select (XCS) and write enable (XWE) before the clock input (CK) rises, and sets the address input (A0 to An) and data input (D0 to Dn). When the clock input rises, the chip select, write enable, address input, and data input signals are all latched, and writing starts. Data written is output from the data output pins (Y0 to Yn) until the clock input rises next.

Reading enables (sets to L) chip select (XCS) and disables (sets to H) write enable (XWE) before the clock input (CK) rises, and sets the address input (A0 to An). When the clock input rises, the chip select, write enable, and address input signals are all latched, and reading starts. Data is output from the data output pins (Y0 to Yn) during this period from when the clock rises until the access time has elapsed.

Table 8-12 Synchronized 1-port RAM Operation Truth Table

CK	XCS	XWE	Output state	Operation mode
L→H	L	H	Read Data	Read
L→H	L	L	Write Data	Write
L→H	H	L or H	Data Hold	Standby

8.4.5 Timing Charts (Synchronous 1-port RAM)

- Read

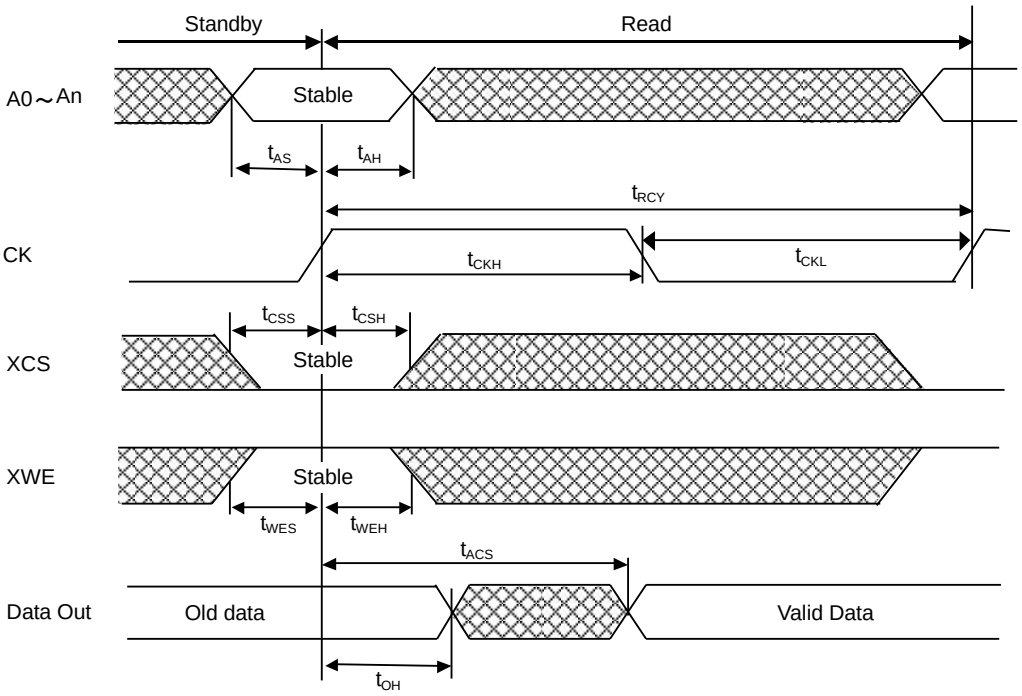


Figure 8-7 Read Cycle

- Write

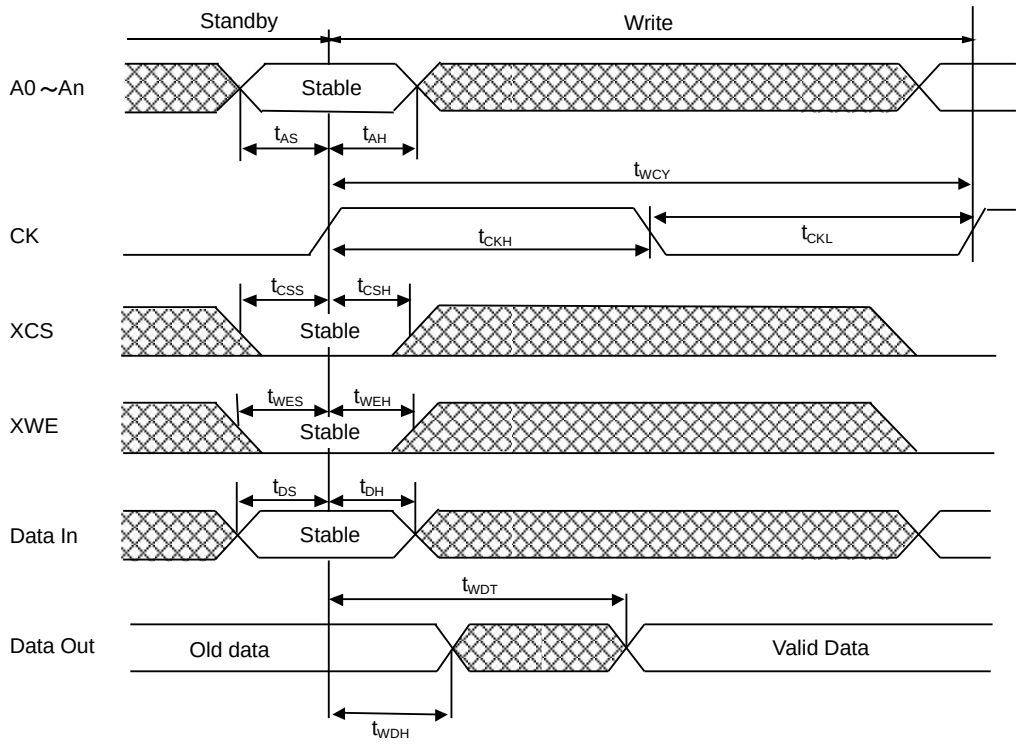


Figure 8-8 Write Cycle

8.5 Synchronous 2-port RAM

8.5.1 Features

(1) Clock synchronized 2-port RAM

(2) Latch circuits for chip select, write enable, address, and data input areas, allowing high-speed operation synchronized with the clock

(3) Separate data input and output ports

(4) 16- to 256-word deep, configurable in 4-word increments
1- to 32-bit wide, configurable in 1-bit increments

(5) Maximum size: 8K bits/module

8.5.2 Word-Bit Configurations and RAM Cell Names

Table 8-13 shows RAM cell names corresponding to typical word-bit configurations. The RAM cells are named in accordance with the following rule, depending on the word-bit configuration.

2-port RAM: "V2S XXX YY" where "XXX" is the word depth (hexadecimal) and "YY" is the bit count (hexadecimal).

Table 8-13 Synchronous 2-port RAM Cell Names According to Word-Bit Configuration

Word depth \ Bit count	4 bits	8 bits	16 bits	32 bits
32 words	V2S02004	V2S02008	V2S02010	V2S02020
64 words	V2S04004	V2S04008	V2S04010	V2S04020
128 words	V2S08004	V2S08008	V2S08010	V2S08020
256 words	V2S10004	V2S10008	V2S10010	V2S10020

8.5.3 RAM Size Estimation

Use the following formulas for estimating the BC count for X and Y directions:

X direction size: RX = (Word depth ÷ 4) × 7 + 32
Y direction size: RY = Bit count × 2 + 9 + α
BC count: RAMBCS = RX × RY
Where α is 4 when 16 ≤ word depth ≤ 32 and 6 when 36 ≤ word depth ≤ 256

Table 8-14 Synchronous 2-port RAM Configuration Examples and BC Count

Word depth \ Bit count	4 bits	8 bits	16 bits	32 bits
32 words	1,848 (88 × 21)	2,552 (88 × 29)	3,960 (88 × 45)	6,776 (88 × 77)
64 words	3,312 (144 × 23)	4,464 (144 × 31)	6,768 (144 × 47)	11,376 (144 × 79)
128 words	5,888 (256 × 23)	7,936 (256 × 31)	12,032 (256 × 47)	20,224 (256 × 79)
256 words	11,040 (480 × 23)	14,880 (480 × 31)	22,560 (480 × 47)	37,920 (480 × 79)

8.5.4 Function Descriptions

(1) I/O signals

Port 1 is used for writing only. Port 2 is used for reading only. Each port has its own clock input pin to allow operation with separate frequencies and timing.

The RAM will be in standby state when write enable (XWA) for port 1 and read enable (XRB) for port 2 are both latched at "H".

Table 8-15 Synchronous 2-port RAM Signal Descriptions

Port 1 synchronous signal (write only)

I/O signal		Function description
Symbol	Name	
CKA	Clock input	Latches write enable (XWA), address input (AA0 to AAn), and data input (D0 to Dn) at the clock input (CKA) rising edge (L → H) and retains inside RAM.
XWA	Write enable	Latched at the clock input (CKA) rising edge. Write operation starts when the latched value is L.
AA0 to AAn	Address input	Latched at the clock input (CKA) rising edge.
D0 to Dn	Data input	Latched at the clock input (CKA) rising edge. Writes to the memory cell when write enable (XWA) is L.

Port 2 signal (read only)

I/O signal		Function description
Symbol	Name	
CKB	Clock input	Latches read enable (XRB) and address input (AB0 to ABn) at the clock input (CKB) rising edge (L → H) and retains inside RAM.
XRB	Read enable	Latched at the clock input (CKB) rising edge. Read operation starts when the latched value is L.
AB0 to ABn	Address input	Latched at the clock input (CKB) rising edge.
Y0 to Yn	Data input	Data is output from the memory cell once the access time has elapsed after the clock input (CKB) rising edge.

(2) Operation description

Writing enables (sets to L) write enable (XWA) before the clock input (CKA) rises, and sets the address input (AA0 to AAn) and data input (D0 to Dn). When the clock input (CKA) rises, the write enable (XWA), address input (AA0 to AAn), and data input (D0 to Dn) signals are all latched, and writing starts.

Reading enables (sets to L) read enable (XRB) before the clock input (CKB) rises, and sets the address input (AB0 to ABn). When the clock input (CKB) rises, the read enable (XRB) and address input (AB0 to ABn) signals are all latched, and reading starts. Data is output from the data output pins (Y0 to Yn) during this period from when the clock input (CKB) rises until the access time has elapsed.

Table 8-16 Synchronized 2-port RAM Operation Truth Table

(Port 1 (write only) operation truth table)

CKA	XWA	Operation mode
L→H	H	Standby
L→H	L	Write

(Port 2 (read only) operation truth table)

CKB	XRB	Output state	Operation mode
L→H	H	Data Hold	Standby
L→H	L	Read Data	Read

Note that if writing and reading are performed simultaneously on the same memory, data will be written to the memory, but the data read out will be unknown.

8.5.5 Timing Charts (Synchronous 2-port RAM)

(1) Port 1

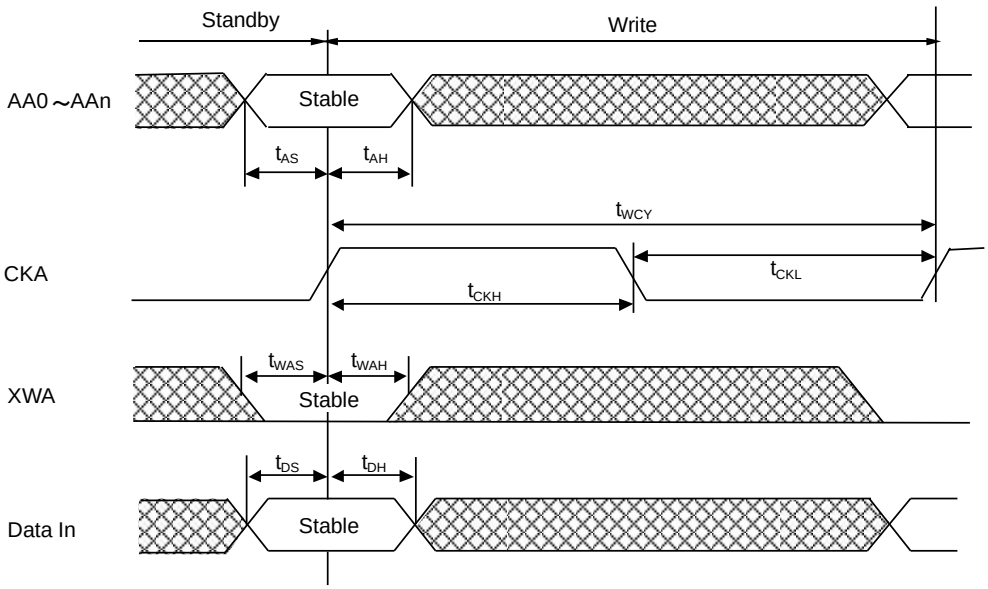


Figure 8-9 Write

(2) Port 2

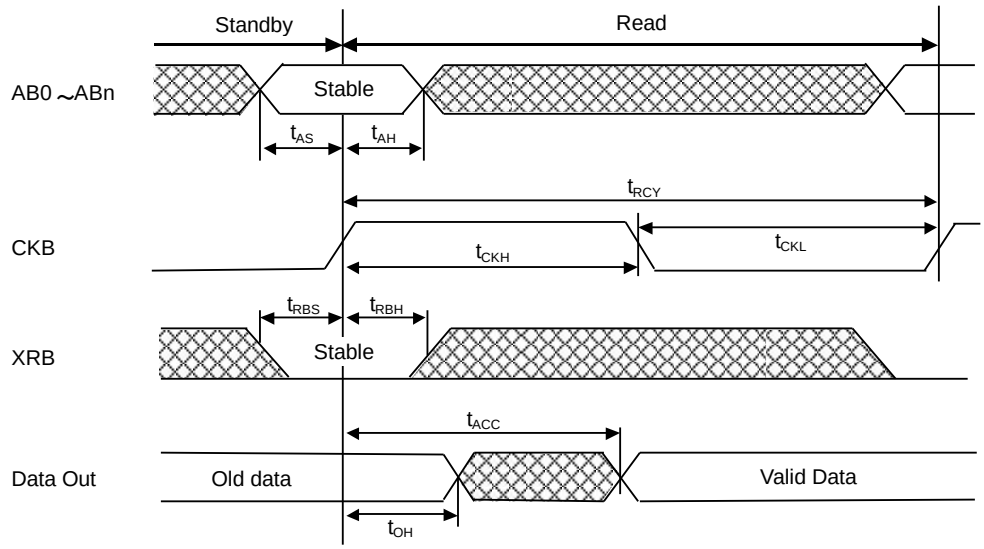


Figure 8-10 Read

8.6 Synchronous RAM Delay Parameters

8.6.1 5.0V Specifications (V_{DD} = 4.5 to 5.5V, T_a = -40 to 110°C)

Table 8-17-1 Synchronous 1-port/2-port RAM Read Cycle (1/2)

Parameter	Symbol	64word x 16bit V1S/V2S04010		64word x 32bit V1S/V2S04020		128word x 16bit V1S/V2S08010		128word x 32bit V1S/V2S08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS} t_{ACC}	—	11.3	—	11.6	—	14.5	—	14.8	ns
Read cycle time	t_{RCY}	11.3	—	11.6	—	14.5	—	14.8	—	
Clock high pulse width	t_{CKH}	1.2	—	1.2	—	1.2	—	1.2	—	
Clock low pulse width	t_{CKL}	1.2	—	1.2	—	1.2	—	1.2	—	
XCS setup time	t_{CSS}	2.6	—	2.6	—	2.6	—	2.6	—	
XCS hold time	t_{CSH}	0.0	—	0.0	—	0.0	—	0.0	—	
XWE setup time	t_{WES}	2.6	—	2.6	—	2.6	—	2.6	—	
XWE hold time	t_{WEH}	0.0	—	0.0	—	0.0	—	0.0	—	
XRB setup time	t_{RBS}	2.6	—	2.6	—	2.6	—	2.6	—	
XRB hold time	t_{RBH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address setup time	t_{AS}	2.6	—	2.6	—	2.6	—	2.6	—	
Address hold time	t_{AH}	0.0	—	0.0	—	0.0	—	0.0	—	
Output hold time	t_{OH}	1.5	—	1.6	—	1.5	—	1.6	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-17-1 Synchronous 1-port/2-port RAM Read Cycle (2/2)

Parameter	Symbol	192word x 16bit V1S/V2S0C010		192word x 32bit V1S/V2S0C020		256word x 16bit V1S/V2S10010		256word x 32bit V1S/V2S10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS} t_{ACC}	—	17.6	—	17.9	—	20.5	—	20.8	ns
Read cycle time	t_{RCY}	17.6	—	17.9	—	20.5	—	20.8	—	
Clock high pulse width	t_{CKH}	1.2	—	1.2	—	1.2	—	1.2	—	
Clock low pulse width	t_{CKL}	1.2	—	1.2	—	1.2	—	1.2	—	
XCS setup time	t_{CSS}	2.6	—	2.6	—	2.6	—	2.6	—	
XCS hold time	t_{CSH}	0.0	—	0.0	—	0.0	—	0.0	—	
XWE setup time	t_{WES}	2.6	—	2.6	—	2.6	—	2.6	—	
XWE hold time	t_{WEH}	0.0	—	0.0	—	0.0	—	0.0	—	
XRB setup time	t_{RBS}	2.6	—	2.6	—	2.6	—	2.6	—	
XRB hold time	t_{RBH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address setup time	t_{AS}	2.6	—	2.6	—	2.6	—	2.6	—	
Address hold time	t_{AH}	0.0	—	0.0	—	0.0	—	0.0	—	
Output hold time	t_{OH}	1.6	—	1.6	—	1.6	—	1.7	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-17-2 Synchronous 1-port/2-port RAM Write Cycle (1/2)

Parameter	Symbol	64word x 16bit V1S/V2S04010		64word x 32bit V1S/V2S04020		128word x 16bit V1S/V2S08010		128word x 32bit V1S/V2S08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	10.1	—	10.8	—	10.4	—	11.0	—	ns
Clock high pulse width	t_{CKH}	1.2	—	1.2	—	1.2	—	1.2	—	
Clock low pulse width	t_{CKL}	1.2	—	1.2	—	1.2	—	1.2	—	
XCS setup time	t_{CSS}	2.6	—	2.6	—	2.6	—	2.6	—	
XCS hold time	t_{CSH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address setup time	t_{AS}	2.6	—	2.6	—	2.6	—	2.6	—	
XWE setup time	t_{WES}	2.6	—	2.6	—	2.6	—	2.6	—	
XWE hold time	t_{WEH}	0.0	—	0.0	—	0.0	—	0.0	—	
XRA setup time	t_{WAS}	2.6	—	2.6	—	2.6	—	2.6	—	
XRA hold time	t_{WAH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address hold time	t_{AH}	0.0	—	0.0	—	0.0	—	0.0	—	
Data hold time	T_{DH}	0.0	—	0.0	—	0.0	—	0.0	—	
Data setup time	t_{DS}	2.6	—	2.6	—	2.6	—	2.6	—	
Write data hold time	t_{WDH}	2.7	—	2.8	—	2.8	—	2.9	—	
Write data through time	t_{WDT}	—	10.1	—	10.8	—	10.4	—	11.0	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-17-2 Synchronous 1-port/2-port RAM Write Cycle (2/2)

Parameter	Symbol	192word x 16bit V1S/V2S0C010		192word x 32bit V1S/V2S0C020		256word x 16bit V1S/V2S10010		256word x 32bit V1S/V2S10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	10.6	—	11.3	—	11.0	—	11.6	—	ns
Clock high pulse width	t_{CKH}	1.2	—	1.2	—	1.2	—	1.2	—	
Clock low pulse width	t_{CKL}	1.2	—	1.2	—	1.2	—	1.2	—	
XCS setup time	t_{CSS}	2.6	—	2.6	—	2.6	—	2.6	—	
XCS hold time	t_{CSH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address setup time	t_{AS}	2.6	—	2.6	—	2.6	—	2.6	—	
XWE setup time	t_{WES}	2.6	—	2.6	—	2.6	—	2.6	—	
XWE hold time	t_{WEH}	0.0	—	0.0	—	0.0	—	0.0	—	
XRA setup time	t_{WAS}	2.6	—	2.6	—	2.6	—	2.6	—	
XRA hold time	t_{WAH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address hold time	t_{AH}	0.0	—	0.0	—	0.0	—	0.0	—	
Data hold time	T_{DH}	0.0	—	0.0	—	0.0	—	0.0	—	
Data setup time	t_{DS}	2.6	—	2.6	—	2.6	—	2.6	—	
Write data hold time	t_{WDH}	2.9	—	3.1	—	3.0	—	3.1	—	
Write data through time	t_{WDT}	—	10.6	—	11.3	—	11.0	—	11.6	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

8.6.2 3.3V Specifications (V_{DD} = 3.0 to 3.6V, T_a = -40 to 110°C)

Table 8-18-1 Synchronous 1-port/2-port RAM Read Cycle (1/2)

Parameter	Symbol	64word x 16bit V1S/V2S04010		64word x 32bit V1S/V2S04020		128word x 16bit V1S/V2S08010		128word x 32bit V1S/V2S08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS} t_{ACC}	—	20.7	—	21.3	—	27.1	—	27.7	ns
Read cycle time	t_{RCY}	20.7	—	21.3	—	27.1	—	27.7	—	
Clock high pulse width	t_{CKH}	2.3	—	2.3	—	2.3	—	2.3	—	
Clock low pulse width	t_{CKL}	2.3	—	2.3	—	2.3	—	2.3	—	
XCS setup time	t_{CSS}	4.9	—	4.9	—	4.9	—	4.9	—	
XCS hold time	t_{CSH}	0.0	—	0.0	—	0.0	—	0.0	—	
XWE setup time	t_{WES}	4.9	—	4.9	—	4.9	—	4.9	—	
XWE hold time	t_{WEH}	0.0	—	0.0	—	0.0	—	0.0	—	
XRB setup time	t_{RBS}	4.9	—	4.9	—	4.9	—	4.9	—	
XRB hold time	t_{RBH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address setup time	t_{AS}	4.9	—	4.9	—	4.9	—	4.9	—	
Address hold time	t_{AH}	0.0	—	0.0	—	0.0	—	0.0	—	
Output hold time	t_{OH}	2.0	—	2.1	—	2.0	—	2.1	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-18-1 Synchronous 1-port/2-port RAM Read Cycle (2/2)

Parameter	Symbol	192word x 16bit V1S/V2S0C010		192word x 32bit V1S/V2S0C020		256word x 16bit V1S/V2S10010		256word x 32bit V1S/V2S10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS} t_{ACC}	—	33.4	—	33.9	—	39.1	—	39.7	ns
Read cycle time	t_{RCY}	33.4	—	33.9	—	39.1	—	39.7	—	
Clock high pulse width	t_{CKH}	2.3	—	2.3	—	2.3	—	2.3	—	
Clock low pulse width	t_{CKL}	2.3	—	2.3	—	2.3	—	2.3	—	
XCS setup time	t_{CSS}	4.9	—	4.9	—	4.9	—	4.9	—	
XCS hold time	t_{CSH}	0.0	—	0.0	—	0.0	—	0.0	—	
XWE setup time	t_{WES}	4.9	—	4.9	—	4.9	—	4.9	—	
XWE hold time	t_{WEH}	0.0	—	0.0	—	0.0	—	0.0	—	
XRA setup time	t_{RBS}	4.9	—	4.9	—	4.9	—	4.9	—	
XRA hold time	t_{RBH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address setup time	t_{AS}	4.9	—	4.9	—	4.9	—	4.9	—	
Address hold time	t_{AH}	0.0	—	0.0	—	0.0	—	0.0	—	
Output hold time	t_{OH}	2.1	—	2.1	—	2.1	—	2.2	—	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-18-2 Synchronous 1-port/2-port RAM Write Cycle (1/2)

Parameter	Symbol	64word x 16bit V1S/V2S04010		64word x 32bit V1S/V2S04020		128word x 16bit V1S/V2S08010		128word x 32bit V1S/V2S08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	18.9	—	20.2	—	19.5	—	20.6	—	ns
Clock high pulse width	t_{CKH}	2.3	—	2.3	—	2.3	—	2.3	—	
Clock low pulse width	t_{CKL}	2.3	—	2.3	—	2.3	—	2.3	—	
XCS setup time	t_{CSS}	4.9	—	4.9	—	4.9	—	4.9	—	
XCS hold time	t_{CSH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address setup time	t_{AS}	4.9	—	4.9	—	4.9	—	4.9	—	
XWE setup time	t_{WES}	4.9	—	4.9	—	4.9	—	4.9	—	
XWE hold time	t_{WEH}	0.0	—	0.0	—	0.0	—	0.0	—	
XRA setup time	t_{WAS}	4.9	—	4.9	—	4.9	—	4.9	—	
XRA hold time	t_{WAH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address hold time	t_{AH}	0.0	—	0.0	—	0.0	—	0.0	—	
Data hold time	T_{DH}	0.0	—	0.0	—	0.0	—	0.0	—	
Data setup time	t_{DS}	4.9	—	4.9	—	4.9	—	4.9	—	
Write data hold time	t_{WDH}	3.6	—	3.7	—	3.7	—	3.9	—	
Write data through time	t_{WDT}	—	18.9	—	20.2	—	19.5	—	20.6	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

Table 8-18-2 Synchronous 1-port/2-port RAM Write Cycle (2/2)

Parameter	Symbol	192word x 16bit V1S/V2S0C010		192word x 32bit V1S/V2S0C020		256word x 16bit V1S/V2S10010		256word x 32bit V1S/V2S10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	19.9	—	21.2	—	20.6	—	21.7	—	ns
Clock high pulse width	t_{CKH}	2.3	—	2.3	—	2.3	—	2.3	—	
Clock low pulse width	t_{CKL}	2.3	—	2.3	—	2.3	—	2.3	—	
XCS setup time	t_{CSS}	4.9	—	4.9	—	4.9	—	4.9	—	
XCS hold time	t_{CSH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address setup time	t_{AS}	4.9	—	4.9	—	4.9	—	4.9	—	
XWE setup time	t_{WES}	4.9	—	4.9	—	4.9	—	4.9	—	
XWE hold time	t_{WEH}	0.0	—	0.0	—	0.0	—	0.0	—	
XRA setup time	t_{WAS}	4.9	—	4.9	—	4.9	—	4.9	—	
XRA hold time	t_{WAH}	0.0	—	0.0	—	0.0	—	0.0	—	
Address hold time	t_{AH}	0.0	—	0.0	—	0.0	—	0.0	—	
Data hold time	T_{DH}	0.0	—	0.0	—	0.0	—	0.0	—	
Data setup time	t_{DS}	4.9	—	4.9	—	4.9	—	4.9	—	
Write data hold time	t_{WDH}	3.9	—	4.1	—	4.0	—	4.1	—	
Write data through time	t_{WDT}	—	19.9	—	21.2	—	20.6	—	21.7	

NOTE: 1: Use the next size up for G/A RAM for configurations not shown in this table.

8.7 Access to Invalid Addresses

If the RAM has 48- or 88-word deep configuration, access to invalid addresses may occur.
If an invalid address is accessed to read data in the actual IC, all word lines go to the off state and all bit lines go floating. Access to invalid addresses is therefore prohibited for the following reasons:

(1) Read operation with all bit lines floating outputs unknown to all the RAM output bits

(2) Read operation with all bit lines floating generates a current flow path in the circuit. The value of this current varies depending on the RAM size or configuration; but it deviates the IC's dynamic and static current values from the specified values.

In the logic simulation, invalid addresses are checked at the rising time of the clock signal in the read/write operation, and if an invalid address is accessed, a timing error is output.

8.8 Embeddable RAM Size

The X and Y dimensions of the location where a RAM is to be embedded must exceed the RAM size in terms of the number of master basic cells used.

If multiple RAMs are used, they should be placed next to each other. The formula mentioned previously includes the wiring area around the RAM. To determine whether the RAM block is embeddable, simply add the RX and RY sizes.

For information on individual master basic cell counts in the X and Y directions, refer to Table 1-1-1.

Chapter 9 PLL Specifications

The S1L5V000 Series includes three types of masters with built-in PLL. When embedding PLL, select from "1.2.2 Built-in PLL Master Lineup." Note that only 5V power supply voltage types are available.

9.1 Features

- Input frequency: 5MHz to 40MHz
- Output frequency: 20MHz to 135MHz
- Multiplication rate: 2, 3, 4, 6, 8, 9, 10, 12, 14, 16, 18, 20, 22, 24, 26
  Pout = Refck * NN * LL (where Refck * LL < 68MHz)
  NN = 2, 3, 4
  LL = 1 to 16
- Clock accuracy: Peak to peak jitter
  When TVC = 000 (POUT = 20 to 40MHz): Output frequency ±1%
  When TVC = 010 (POUT = 41 to 60MHz): Output frequency ±1.5%
  When TVC = 100 (POUT = 61 to 80MHz): Output frequency ±2%
  When TVC = 110 (POUT = 81 to 130MHz): Output frequency ±3%
  Example: Target frequency ±222ps when Pout = 135MHz
  * Does not include phase matching function.
- Output duty: 50% ±10%
- Consumption current: Condition 1: MCLVDD = AVDD = 5.0V, REFCK = 13MHz →
  POUT = 52MHz (×4) ⇒ Iop1 = 950µA @typ
- Oscillation start time: Max. 100µs from power down reset when input clock is stable
- Low pass filter: Built-in RC filter (external part not required)
- Power-down function (consumption current not exceeding 3µA)

* Output monitor pin: Using the output monitor (VCP) pin as the output pin is recommended for monitoring the PLL operating status.

* Power supply separation: Separating power supplies is recommended to increase noise immunity.

9.2 Block Diagram

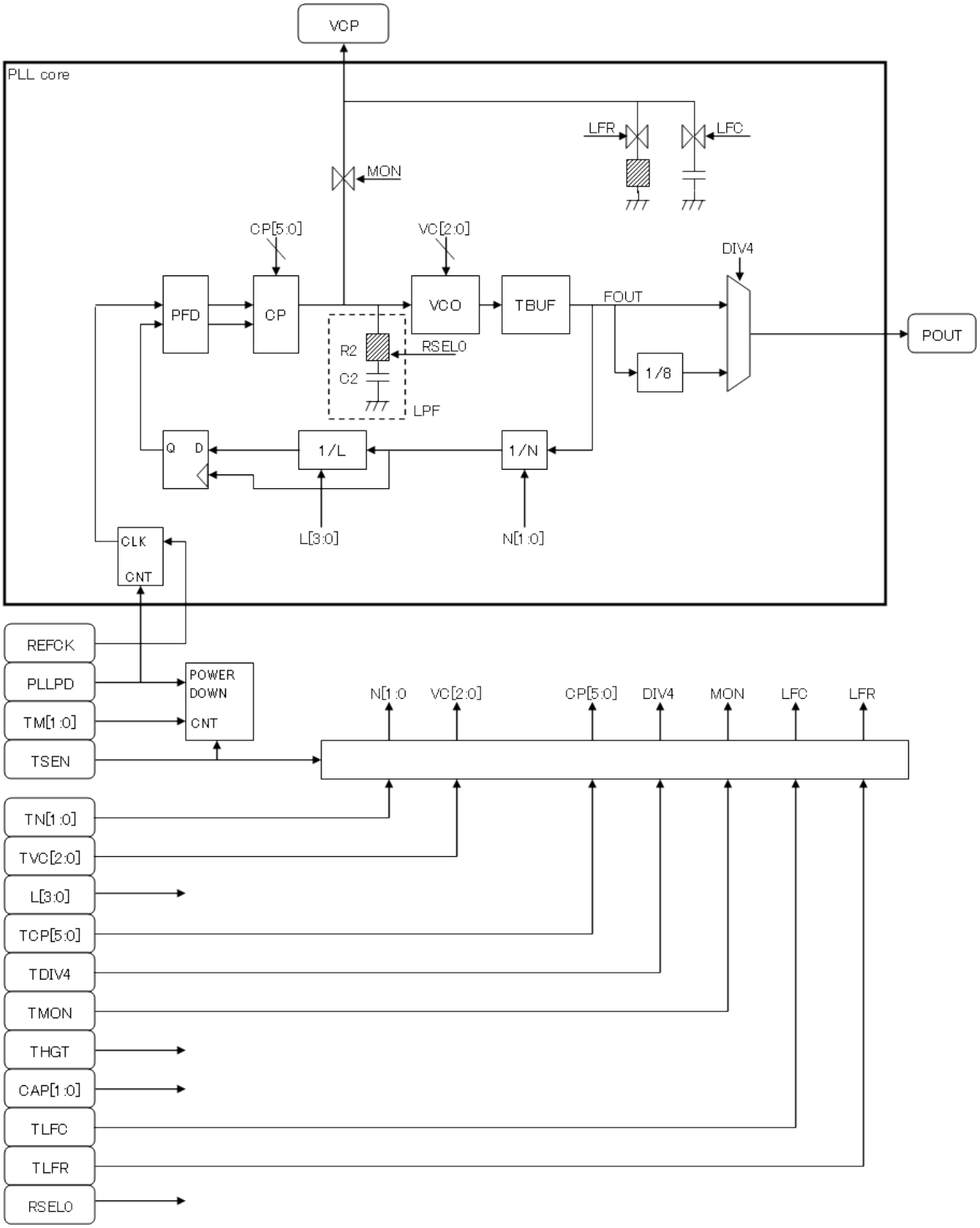


Figure 9-1 PLL Block Diagram

9.3 Pin Functions

Table 9-1 shows the PLL pin attributes.

Table 9-1 PLL Pin List

Signal name	Attribute*1	Function	Comment
MCLVDD MCLVSS AVDD AVSS	P	PLL Digital power supply PLL Digital GND PLL Analog power supply PLL Digital GND	4.5V–5.5V 0V = MCLVDD 0V
Normal Function			
REFCK	I	Reference clock input pin	-
POUT	O	PLL output pin	PLLPD = 1: POUT = Low
PLLPD	I	Power down setting (= reset signal*2)	PLLPD = 0: PLL enable PLLPD = 1: Power down
TSEN	I	Test enable	TSEN = 0: Normal mode TSEN = 1: Test mode
TN[1:0]	I	Multiplication rate setting NN = TN[1:0]+1 (= 2, 3, 4)	eg.) N[1:0] = 11 ⇒ ×4 N[1:0] = 01 ⇒ ×2 N[1:0] = 00 ⇒ Prohibited
L[3:0]	I	Multiplication rate setting LL = L[3:0]+1	eg.) L[3:0] = 1111 ⇒ ×16 L[3:0] = 0000 ⇒ ×1
		Output frequency POUT_freq = REFCK × NN × LL	
TVC[2:0]	I	VCO speed setting	POUT = 20MHz–40MHz ⇒ TVC[2:0] = 000 POUT = 41MHz–60MHz ⇒ TVC[2:0] = 010 POUT = 61MHz–80MHz ⇒ TVC[2:0] = 100 POUT = 81MHz–135MHz ⇒ TVC[2:0] = 110
Test Function			
VCP	AO	Analog monitor output	TMON = 0: Hi-Z, TMON = 1: Monitor
TMON	I	VCP setting	Disabled for TSEN = 0 (Used only for pre-shipment testing)
TM[1:0]	I	Charge pump test setting	
TDIV4	I	POUT division output enable	
TLFC	I	LPF test	Fixed at “0” in normal mode
TLFR	I	LPF test	Fixed at “0” in normal mode
TCP[5:0]	I	Charge pump current setting	Fixed at “11_0100” in normal mode
THGH	I	Lock test	Fixed at “0” in normal mode
CAP[1:0]	I	On-chip LPF setting	Fixed at “10” in normal mode
RSEL0	I	On-chip LPF setting	Fixed at “0” in normal mode

NOTE: *1: P: Power, I: Input, O: Output, AO: Analog output
*2: Be sure to initialize (PLLPD = 1) before starting PLL operation.

9.4 Electrical Characteristics

9.4.1 Operating Conditions

Table 9-2 Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
MCLVDD AVDD	MCLVDD/AVDD reference to MCLVSS/AVSS	4.5	5.0	5.5	V
T_j	Junction temperature	-40	25	135	°C
Vin	Input voltage range	0	—	MCLVDD	V
Fin	Input reference clock frequency	5	—	40	MHz
Fout	PLL output frequency	20	—	135	MHz
Fvco	VCO frequency	20	—	135	MHz

9.4.2 DC Characteristics

Table 9-3 DC Characteristics

(MCLVDD/AVDD = 5.0V ±0.5V, MCLVSS/AVSS = 0V, Tj = -40°C to 135°C)

Item	Symbol	Conditions	Min	Typ	Max	Unit
PLL current	Idd1	Output unloaded, Fin = 13MHz, Fout = 52MHz(×4) TN[1:0] = 11, L[3:0] = 0000	—	950	1280	µA
	Idd2	Output unloaded, Fin = 20MHz, Fout = 120MHz(×6) TN[1:0] = 10, L[3:0] = 0001	—	2600	3150	µA
Power down current	Iq	PLLPD = 1	—		3	µA

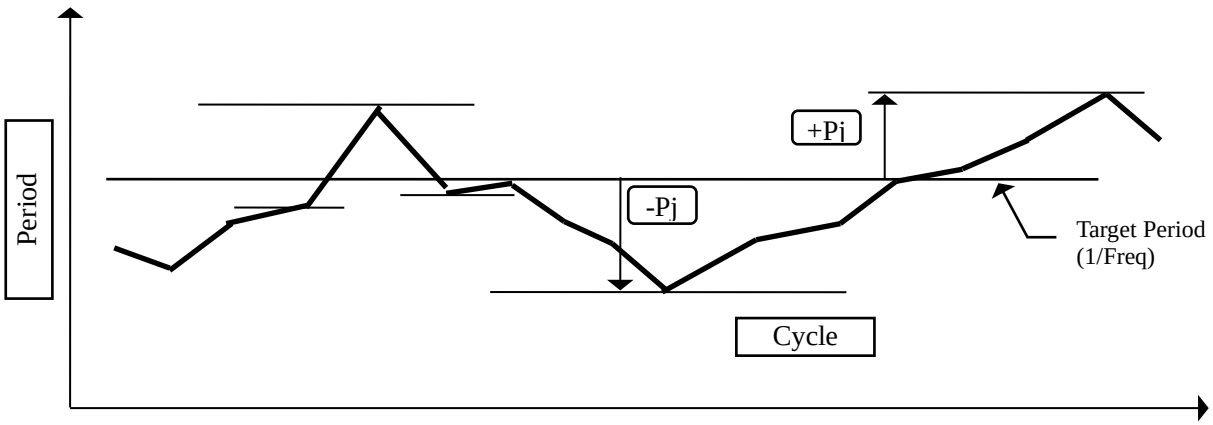
9.4.3 AC Characteristics

Table 9-4 AC Characteristics

(MCLVDD/AVDD = 5.0V ±0.5V, MCLVSS/AVSS = 0V, Tj = -40°C to 135°C)

Item	Symbol	Conditions	Min	Typ	Max	Unit
PLLPD minimum pulse width	Thpd	High pulse width	20	—	—	ns
POUT duty	Duty	CMOS level High_Duty	40	50	60	%
Peak jitter	Pj	TVC = 000 (POUT = 20 to 40MHz)	-1	—	+1	%
		TVC = 010 (POUT = 41 to 60MHz)	-1.5	—	+1.5	
		TVC = 100 (POUT = 61 to 80MHz)	-2	—	+2	
		TVC = 110 (POUT = 81 to 130MHz)*1	-3	—	+3	
Lockup time	Tlock1	from PLLPD = 1→0 release REFCK, MCLVDD and AVDD be stable	—	—	100	µs

NOTE: *1: When peak to peak jitter is the target frequency ±3% (see figure below)
Example: Pout frequency = 135MHz, clock cycle = 7.407ns
"Pj = ±3%" so the clock cycle range will be 7.407ns ±220ps.



9.4.4 Multiplication Rate Setting

Determined by the combination of N_divider (TN[1:0]) and L_Divider (L[3:0])

NN = TN[1:0] + 1, LL = L[3:0] + 1

* Constraints

a) TN[1:0] = 00 is prohibited
b) REFCK * LL < 68MHz
c) 135MHz ≥ POUT_freq ≥ 20MHz

Table 9-5 All Multiplication Rate Settings for REFCK = 10MHz

TN[1:0]	NN	L[3:0]	LL	Multiplication rate (= NN * LL)	REFCK * LL (max. 68MHz)	POUT_freq
01	2	0000	1	2	10MHz	20MHz
01	2	0001	2	4	20MHz	40MHz
01	2	0010	3	6	30MHz	60MHz
01	2	0011	4	8	40MHz	80MHz
01	2	0100	5	10	50MHz	100MHz
01	2	0101	6	12	60MHz	120MHz
10	3	0000	1	3	10MHz	30MHz
10	3	0001	2	6	20MHz	60MHz
10	3	0010	3	9	30MHz	90MHz
10	3	0011	4	12	40MHz	120MHz
11	4	0000	1	4	10MHz	40MHz
11	4	0001	2	8	20MHz	80MHz
11	4	0010	3	12	30MHz	120MHz

* For example, while there are three possible setting methods if the multiplication rate is 12, electrical characteristics such as jitter, lockup time, and output duty will be the same. The consumption current however may differ slightly.

Table 9-6 All Multiplication Rate Settings for REFCK = 40MHz

TN[1:0]	NN	L[3:0]	LL	Multiplication rate (= NN * LL)	REFCK * LL (max. 68MHz)	POUT_freq
01	2	0000	1	2	40MHz	80MHz
01	2	0001	2	4	80MHz	Prohibited by constraint b)
10	3	0000	1	3	40MHz	120MHz

* If the constraints are not met, the PLL will output a clock that cannot be guaranteed.

Chapter 10 Calculating Total Power Consumption

The power consumption values calculated in this chapter are not guaranteed figures and should be used strictly for reference purposes. Calculate power consumption as a reference for determining whether the power consumption is within the allowable range.

10.1 Calculating Power Consumption

The power consumption is dependent on operating frequency, load capacitance, and power supply (except in special cases involving steady-state currents, such as special macros).

To estimate IC total power consumption, obtain the power consumption of each block in the internal circuit first, and add them up. Then obtain the power consumption of input and output buffers, and add up these values, too.

10.1.1 Internal Cells (P_{int})

The internal circuit power consumption P_{int} is calculated as the sum of the internal circuit area power consumption calculated for each block.

(1) Power consumption P_{BC} when internal circuits are logic circuits only

$$P_{int} = P_{BC} = \sum_{i=1}^{K} (Nb \times fi \times Spi \times Kpint) \ [\mu W]$$

where
Nb: Total BC count for circuits operating at fi [MHz]
fi: Operating frequency [MHz]
Spi: Proportion of BCs out of Nb operating simultaneously at fi [MHz]
Example: Spi = 1.0 when all circuits operate simultaneously at fi [MHz]
Spi = 0.5 when 50% of circuits operate at fi [MHz] due to block division
Kpint: Power consumption per BC

Table 10-1 shows the power consumption values per BC (Kpint).

Table 10-1 Kpint per BC for S1L5V000 Series

V_{DD} (TYP)	Kpi
5.0V	1.30µW/MHz
3.3V	0.54µW/MHz

(2) If RAM blocks are used

$$P_{int} = P_{BC} + P_{BM}$$

where
P_{BC}: Power consumption for basic cell area
P_{BM}: RAM power consumption

For information on RAM power consumption, please contact our sales representative, indicating the bit-word configuration.

10.1.2 Input Buffers (P_i)

The power consumption for input buffers is the sum of the frequency f [MHz] of the signal input to each buffer multiplied by Kpi [µW/MHz].

$$P_i = \sum_{i=1}^{K} (Kpi \times fi) \ [\mu W]$$

fi: Ith input buffer operating frequency [MHz]
Kpi: Input buffer voltage coefficient (See Table 10-2.)

Table 10-2 S1L5V000 Series Input Cell Kpi

V_{DD} (TYP)	Kpi
5.0V	17.7µW/MHz
3.3V	6.2µW/MHz

10.1.3 Output Buffers (P_o)

The power consumption for output buffers will differ between DC loads (resistance loads: for example, when a TTL device is connected) and AC loads (capacitance load: for example, when a CMOS device is connected).

If the DC power consumption is P_{DC} and the AC power consumption is P_{AC}, the power consumption P_o for the output buffer can be calculated using the following formula:

$$P_o = P_{AC} + P_{DC}$$

(1) AC power consumption (P_{AC})

The power consumption with an AC load can be estimated using the following formula:

$$P_{AC} = \sum_{i=1}^{K} \{fi \times C_L \times (V_{DD})^2\}$$

where
fi: Output buffer operating frequency [Hz]
C_L Output load capacitance [F]
V_{DD}: Power supply voltage [V]

(2) DC Power Consumption (P_{DC})

Approximate DC power consumption is obtained by the following formula:

$$P_{DC} = P_{DCH} + P_{DCL}$$

$$P_{DCH} = |I_{OH}| \times (V_{DD} - V_{OH})$$

$$P_{DCL} = I_{OL} \times V_{OL}$$

Here, the ratio of P_{DCH} to P_{DCL} is determined by the duty ratio of output signal.

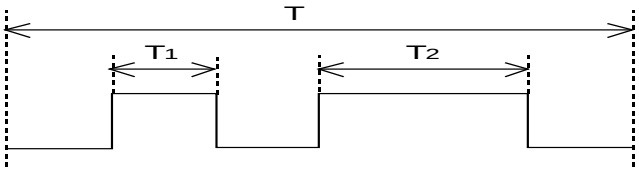


Figure 10-1 Duty Cycle Example

In Figure 10-1,

Duty H = $(T_1 + T_2) \div T$
Duty L = $(T - T_1 - T_2) \div T$

Therefore

$$P_{DC} = P_{DCH} + P_{DCL}$$
$$= \sum_{i=1}^{K} \{(V_{DD} - V_{OH}i) \times I_{OH}i \times \text{Duty H}\} + \sum_{i=1}^{K} [V_{OL}i \times I_{OL}i \times \text{Duty L}]$$

10.2 Limit on Power Consumption

The chip temperature will increase with power consumption. The IC delay will also vary depending on the IC chip junction temperature Tj. Standard IC specifications are indicated using Ta, but the correlation between Tj and Ta is not constant, and will vary depending on the thermal resistance and power consumption for that IC package.

The IC chip temperature can be calculated as follows from the ambient temperature Ta, package thermal resistance θj-a, and power consumption PD. For the thermal resistance of each package, refer to our web site: www.global.epson.com/products_and_drivers/semicon/products/asic/package_list.html#ac06.

Chip temperature (Tj) = Ta + ($P_D \times \theta$j-a) (°C)

Specifications are normally stipulated using Ta, so the delay library is provided using the following guide:

* For Ta = -40 to 110 [°C], Tj = -40 to 135 [°C] library

Please note that Epson may add other conditions in cases in which the correlation between Ta and Tj varies significantly depending on the package and estimated power consumption.

Use the S1L5V000 Series with a chip temperature (Tj) not exceeding 135°C.

Appendix

A1. Simulation Results Example

A1.1 Comparison File Example for Simulation Results and Expected Values

```
# APF file comparison program (apfcomp)
# version 2.70 Copyright (c) 1995-2003. SEIKO EPSON CORPORATION
#       EXPECT        : samp.apf                    ← Expected value file name to be compared
#       COMPARE       : samp.sammax                 ← APF file name to be compared
#       RESULT        : samp.expmax                 ← Comparison results file
#       RUN DATE      : Wed Feb 13 15:03:14 2008    ← Program run date/time
#       DON'T CARE :                                ← "X" if "-noxcare" option was specified; "." if "-nodotcare" was specified
#       IGNORE RZ     : NO                          ← "YES" if "-norzcare" was specified
#
$DESIGN    sample

$RATE    100000
$STROBE    98000
$RESOLUTION    0.001ns

$IOCONT
I_14.E    E0    DATA3
I_15.E    E0    DATA2
I_16.E    E0    DATA1
$ENDIOCONT

$NODE
SEL       I     0
CK        N     0    50000
RESET     I     0
DATA1     BU    0
DATA2     BU    0
DATA3     BU    0
$ENDNODE
# Compared      ......

$PATTERN
#                 SCRDDD
#                 EKEAAA
#                 L STTT
#                    EAAA
#                    T123
#
#                 INIBBB
#                     UUU
#
             3    0N0LLL
#Mismatch             H                              ← Mismatch line and mismatch value
            10    0N1LLH
#Mismatch             HX                             ← Mismatch line and mismatch value
            12    0N1LHL
#Mismatch             H ?                            ← Mismatch line and mismatch value
$ENDPATTERN
#         3 Mismatch lines found.    93.2% Matched    ← Number of mismatch lines and matched percentage within pattern
# End event of EXPECT_file    = 43                   ← End event of expected value file
# End event of COMPARE_file = 43                     ← End event of APF file
# MISMATCH SIGNAL         Actual / Total number of mismatches at each node.
# * Actual = Total number of mismatches at each node minus(-) number of "?".
# <<    DATA1       >>        COUNT =        3/3     ← Mismatch signal name and number of mismatches
# <<    DATA2       >>        COUNT =        1/1          Number of mismatches excluding COUNT=? out of total mismatches
# <<    DATA3       >>        COUNT =        0/1
```

Mismatches arising in the comparison file may be due to the following causes:

(1) Flip-flop mismatch
Note that errors will not appear on the timing error list if the setup time or hold time constraints are exceeded.

(2) Strobe point exceeded due to output delay
This may occur in cases in which the output results from one output pin appear to change constantly with a delay corresponding to one cycle from the expected output value. The delay may occur for L output or H output only.

(3) Combination circuit hazard at output end stage
Hazards (glitches, spike pulses) occurring in combination circuits may be output externally. This can be confirmed in the NARROW report on the timing error list. To avoid this, signals from combination circuits should first be received using a flip-flop before being output.

(4) Unknown value (X) propagation
The RAM and flip-flop output is unknown before initialization.
If combination circuits exist on the clock line, the flip-flop output will be unknown if hazards occurring due to variations coinciding with input are input to that flip-flop clock pin.
Likewise, if a composite cell for clock gating (e.g., CLPSAD2X4) is inserted using Power Compiler or similar tool, the output clock will be unknown if an unknown signal is input to the enable pin.

A1.2 Timing Error List

A list (*.errmax, *.errmin) like that shown in Figure A1-1 is output if a timing error occurs during simulation. This section describes how to read the timing list in conjunction with Figure A1-2.

```
*
*OUTPUT NAME VALUE OFFSET/EVENT NUMBER
**--------------------------------------------------------------------------------
I=top.ffreg1_reg(a) (D ->posedge C &&& (VM6 != 0)(b) ==SETUP TIME ERROR(c) ...SPEC =325(d) )
323(e) 471(f)/   3 35 120 185(g)
**-------------------------------------------------------------------SUB_TOT 4(h)
I=top.ffreg5_reg (posedge C ->D ==HOLD TIME ERROR ...SPEC =106 )
93 474/     3
**-------------------------------------------------------------------SUB_TOT 1
I=top.sub1.flag_a_0 (negedge R ->posedge C &&&(D !==0)  ==SETUP TIME ERROR ...SPEC =334 )
320 482/   3 276
309 482/   405
309 419/   797 961 1221 1477 1649 3017
309 447/   2722
**-------------------------------------------------------------------SUB_TOT 10
*-------------------------------------------------------------------TOTAL 15(i)
```

Figure A1-1 Timing Error List Example

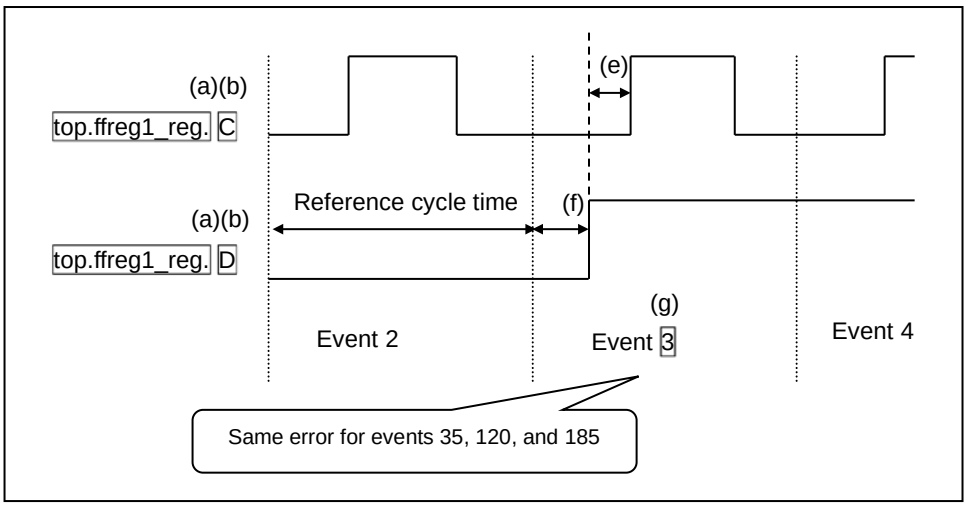


Figure A1-2 Illustration with Waveform

(a) Timing error instance name

Displays the instance name for the timing error as a full path.

In the case shown in the example of Figure A1-1, the error instance name is the FF “top.ffreg1_reg”. The instance name can be used to determine whether the timing error constitutes a problem location. Note that the instance name may change during logic synthesis.

(b) Timing error detection conditions

The specific conditions under which a timing error occurs.

“A ->B&&&(C)” indicates that “B changes after A changes under condition C”.

In the case shown in the example of Figure A1-1, the condition corresponds to “A rising signal is input to pin C after the pin D signal changes while flag VM6 is at a state other than 0”. “VM*” indicates the timing error detection flag in the cell (FF in this case) simulation model. Ignore this if the condition statement is “VM*”. In this example, check only the relationship between pins C and D.

If “NARROW*” is indicated, refer to the description from “MINIMUM PULSE WIDTH” onward in (c) below.

(c) Types of timing constraints

The following are the major types of timing constraints causing errors:

SETUP TIME:	Setup time constraint
HOLD TIME:	Hold time constraint
MINIMUM PULSE WIDTH:	Minimum pulse width constraint

“NARROW*” may be indicated in section (b). This indicates that the length is 75% or less of the rate (reference cycle time), since it is difficult to check the output waveform in detail when checking simulation results using the sampled data (APF). The “NARROW*” indication does not necessarily mean that this error must be fixed. Check the circuit specifications to determine that this causes no issues.

(d) Timing error detection standards (units: ps)

The minimum value for which no error occurs

In the example shown above, an interval of at least 325ps must be left between the “D” change and “posedge C” to prevent a SETUP error from occurring.

(e) Actual timing value (units: ps)

In the example shown above, the SETUP constraint was short by 2ps (= 325ps − 323ps).

(f) Timing error offset (units: ps)

The time from event start until an error occurs

In the case shown in the example of Figure A1-1, this indicates that a timing error occurred 471ps after the event start.

(g) Timing error event (cycle) number

This lists the event numbers for which timing errors have occurred. In the case shown in Figure A1-1, errors have occurred for event numbers 3, 35, 120, and 185. Check against the simulation results to determine whether this constitutes a problem with circuit specifications.

(h) Timing error subtotal

Number of timing errors with the same instance name, error detection conditions, and timing constraints

(i) Timing error total

Total number of timing errors

A2. RTL Design Restrictions and Limitations (VHDL)

As described in section 1.5.3, provisional circuit data provided by the customer can be used to identify problems in the RTL description in advance. However, depending on the description, errors may also be detected in locations not intended by the customer. Circuits should be designed in accordance with the general RTL design style guide to avoid such issues.

A2.1 Provision of RTL Supporting Logic Synthesis

The RTL provided should use only descriptions that allow logic synthesis. Logic synthesis is not possible if behavior level descriptions are included. If the description supports logic synthesis, splitting into separate files should not give rise to problems.

A2.2 Provision of Hierarchical Design Diagrams

The module may be a hierarchical design. If a hierarchical design is used, please send hierarchical structure diagrams (tree diagrams) or documentation showing the hierarchical relationship between modules.

A2.3 RAM Description

Epson does not provide support for RAM VITAL models. Only Verilog models can be provided. If you need a Verilog model, please specify the required RAM size and quantities. Please note that providing RAM Verilog models may take several days.

If RAM models are described by the customer, please ensure that these comply with the specifications described in "Chapter 8 RAM Specifications" of the Design Guide. Additionally, provide module names for the model.

A2.4 Constant Assignment to Input Ports

Constants cannot be assigned directly to input ports using the port_map statement. Likewise, it is not possible to assign "open" or to omit the description. Otherwise, errors will occur during logic synthesis. To avoid this, map "signal" with a constant.

```
Architecture BEHAVIOR of example3_4
signal dummy0 std_logic;
signal dummy1 std_logic;
begin
  dummy0 <= 0;
  dummy1 <= 1;
port map abcx ( a => dummy0, b=> dummy1, c=> data_in, x => data_out )
end BEHAVIOR;
```

Figure A2-1 Mapping "signal" with a Constant

A2.5 Pin Name Constraints

We recommend that the names of external and internal pins conform to the constraints described in the design guide. Please note that names that fail to comply with the constraints may be changed to unintended names during logic synthesis.

(1) External pin name constraints

① Describe entirely in upper case.

② Only alphanumeric characters and the underscore ("_") character can be used.
The first character must be a letter of the alphabet and the last character must be an alphanumeric character.

③ The underscore ("_") character cannot be used in succession.

④ Names must be two to 32 characters long.

⑤ "read" and "write" are not reserved words but cannot be used (for system use).

(2) Internal pin name constraints

① Names may include both upper and lower case characters. However, identical names cannot be used if they differ by upper or lower case.
Example: "ABC" and "Abc" cannot be used at the same time.

② Alphanumeric characters, the underscore ("_") character, and parentheses "(" and ")" for bus descriptions can be used.

③ Names must be two to 32 characters long.

(3) VHDL reserved words

The following text strings cannot be used as user-defined names:

abs	access	after	alias	all	and	architecture
array	assert	attribute	begin	block	body	buffer
bus	case	component	configuration	constant	disconnect	downto
else	elsif	end	entity	exit	file	for
function	generate	generic	guarded	if	in	inout
is	label	library	linkage	loop	map	mod
nand	new	next	nor	not	null	of
on	open	or	others	out	pakage	port
procedure	process	range	record	register	rem	report
return	select	severity	signal	subtype	then	to
transport	type	units	until	use	variable	wait
when	while	with	xor			

(4) Verilog-HDL reserved words

VHDL-RTL needs to be converted to Verilog netlists for compatibility with the tools used in the work carried out at Epson.

Thus, the following text strings cannot be used as user-defined names:

always	and	assign	begin	buf	bufif0	bufif1
case	casex	casez	cmos	deassign	default	defparam
disable	edge	else	end	endcase	endmodule	endfunction
endprimitive	endspecify	endtable	endtask	event	for	force
forever	fork	function	highz0	highz1	if	ifnone
initial	inout	input	integer	join	large	macromodule
medium	module	nand	negedge	nmos	nor	not
notif0	notif1	or	output	parameter	pmos	posedge
primitive	pull0	pull1	pullup	pulldown	rcmos	real
realtime	reg	release	repeat	rnmos	rpmos	rtranif0
rtranif1	scalared	small	specify	specparam	strong0	strong1
supply0	supply1	table	task	time	tran	tranif0
tranif1	tri	tri0	triand	trior	trireg	vectored
wait	wand	weak0	weak1	while	wire	wor
xnor	xor					

A2.6 Port Data Format

Only the std_logic data format can be used for the uppermost module ports. Bus descriptions are not permitted. Use std_logic and std_logic_vector for all other module ports. Note that bus descriptions may be expanded during logic synthesis at Epson.

A2.7 “integer” Usage

Care is required with the bit width when using “integer”. We recommend making “signal” declarations using std_logic_vector, then converting with conv_integer when calculating.

A2.8 I/O Buffers

I/O buffers will be added at Epson. Please provide pinout tables specifying buffer types and output load capacitances. If the timing conditions are exacting or if special buffers such as fail-safe buffers are used, specify this when submitting the provisional data.

The top module of I/O buffers can be safely and easily changed from an RTL type to a gate type. A top module for gate use will be created at Epson. The customer only need include descriptions related to input and output in the RTL top module. More specifically, uni-directional ports should only be connected to lower modules on a one-to-one basis. Bi-directional ports should include description for bi-directional signals within the top module extracting the input signal ports, output signal ports, and enable signal ports from the lower layers.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
entity TOP is
   port( IN1 : in std_logic;    OUT1 : out std_logic;    BID1 : inout std_logic);
end TOP;

architecture rtl of TOP is
   signal en, bid1_out : std_logic;
   component CORE
      port( in1, bid1_in             : in    std_logic ;
            out1, bid1_out, en : out std_logic    );
   end component;

begin
      U_CORE : CORE port map( in1 => IN1, out1 => OUT1, bid1_in => BID1,
                                          bid1_out => bid1_out, en => en);
      BID1 <= 'Z' when en = '1' else bid1_out ;
end rtl;

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity CORE is
   port( in1, bid1_in             : in    std_logic ;
         out1, bid1_out, en : out std_logic    );
end CORE;

architecture rtl of CORE is
begin
end rtl;
```

Figure A2-2 Top Module RTL Example

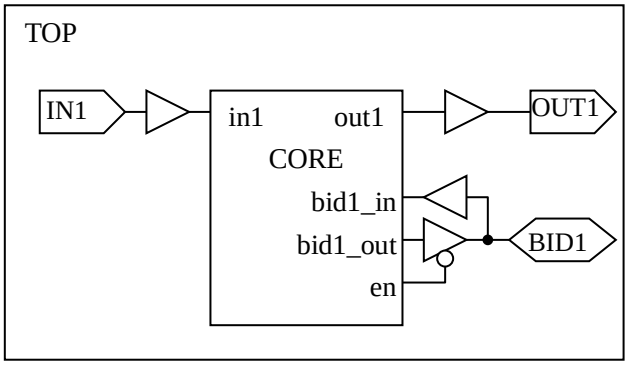


Figure A2-3 Top Module Schematic

A2.9 Primitive Cell Usage

Please notify us of module names within the RTL calling up Epson primitive cells as well as the primitive cell names. The settings will be configured to ensure that primitive cells are not deleted during logic synthesis. Additionally, delete statements related to Epson libraries described during simulation. Asynchronous RAM model library statements should also be deleted.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

----- comment out -----
-- library S1L50000_TYP,S1L50000_RAM;
-- use S1L50000_TYP.all;
-- use S1L50000_TYP.all;
----- comment out -----
```

Figure A2-4 Commenting Out Epson Library Statements

A3. AC/DC Test Patterns

A3.1 DC Test Patterns

The following test items should be taken into consideration if the customer prepares DC test circuits.

DC testing verifies the DC characteristics of the IC. The test makes its measurements at the end of a test event. The pins tested should remain in the same state in the test event after the strobe.

The following DC characteristics are measured:

(1) Static current (I_{DDS}) test

Static current is leakage current that flows through the IC power supplies when input signals are stable. This leakage current is normally extremely small and must be measured with no other currents flowing. All of the following conditions must be met to achieve this. Additionally, there must be at least two events in which the static current is measurable.

① All input pins must be stable.

② There must be high or low level input or output to/from bi-directional pins.

③ There must be no active elements such as oscillators in the circuit.

④ Internal 3-state buffers (internal bus) must be neither floating nor in contention.

⑤ Current must not be flowing through function cells such as RAM.

⑥ There must be high level input to input pins with pull-up resistors.

⑦ There must be high level input or output to/from bi-directional pins with pull-up resistors.

⑧ Bi-directional pins with pull-down resistors must be in the input state or outputting low level.

(2) Input current test

This tests parameters related to the input of input buffers, including input leakage current and pull-up and pull-down currents. The test measures the current flowing when V_{DD} or V_{SS} level voltage is applied to the target pin. That is, either high or low level voltage is applied to the pins under test.

For example, if a V_{DD} level (high level) voltage is applied to a target pin with a low level voltage applied, the target pin state will change from low to high, and the IC may behave unexpectedly.

To test the input current, the V_{DD} level voltage is applied to the target pin in an event in the test pattern in which the pin is subjected to high input, and the V_{SS} level voltage is applied in an event in which the pin is subjected to low input. These target pin states must therefore exist in the test patterns to enable testing.

Input current testing is further subdivided into the following tests:

(3) Input leakage current test (I_{IH}, I_{IL})

This tests parameters related to the input current of input buffers without pull-up or pull-down resistors.

The current that flows when high level voltage is applied to the input buffer is called I_{IH}. This is guaranteed up to the maximum current. Test patterns for this test must contain events with high level input to the pins under test. In the case of bi-directional pins, there must be high level input while in the input state.

The current that flows when low level voltage is applied to the input buffer is called I_{IL}. This is guaranteed up to the maximum current. Test patterns for this test must contain events with low level input to the pins under test. In the case of bi-directional pins, there must be low level input while in the input state.

(4) Pull-up current test (I_{PU})

This measures the current flowing when the low level voltage is applied to an input buffer with a pull-up resistor. Test patterns for this test must contain events in which low level signals are input to the pins under test. In the case of bi-directional pins, low level signals must be input while in the input state.

(5) Pull-down current test (I_{PD})

This measures the current flowing when the high level voltage is applied to an input buffer with a pull-down resistor. Test patterns for this test must contain events with high level input to the pins under test. In the case of bi-directional pins, there must be high level input while in the input state.

(6) Output characteristics test (V_{OH}, V_{OL})

This tests the current drivability of output buffers. With the test pins driven to the target output level, the voltage drop is measured when the specified current load is applied.

To test the output characteristics, the test patterns must include all possible target pin states. Also, those states must remain unchanged during the test event even if the test rate is indefinitely extended.

(7) Off-state leakage current (I_{OZ})

This measures the leakage current that flows to an open drain or 3-state output buffer when the output state is high impedance. It actually measures the current when the V_{DD} level or V_{SS} level voltage is applied to the test pins in the high impedance state. This means the test patterns must contain events in which the test pins are in the high impedance state.

A3.2 AC Test Patterns

AC testing measures the time taken for a signal change occurring in an input pin to propagate to an output pin. If the customer prepares the AC test circuit, the customer should select the AC test path.

(1) Constraints on test events

This test method is typically performed by the binary search method. The target test pin (output pin subject to change) must have only a single change point within a test event. (Pins that output RZ waveforms cannot be tested. Pins that output hazard in the test event cannot be tested, either.) The tested signal changes must be “High” to “Low” or “Low” to “High.” (Changes related to Z cannot be tested.)

Take care to avoid selecting test events in which multiple output signals change simultaneously or bi-directional and IC tester signals are in contention. The presence of simultaneous signal changes or signal contention destabilizes the IC power supply, affecting the output waveforms of the test pins and preventing accurate testing.

(2) Constraints on AC test points

The number of AC test points must be four or fewer.

(3) Constraints on test path delay

Testing accuracy increases with increased test path delay. Set the test path delay to at least 30ns and less than the strobe point for the test simulation maximum condition.

(4) Other constraints

① Do not specify paths from oscillator circuits.

② Specify paths not passing through the internal 3-state circuit (internal bus).

③ Do not specify paths passing through other bi-directional buffers between the test path input buffer and an output buffer.

④ If the IC has multiple operating voltage ranges, test within one voltage range.

(5) Constraints on bi-directional pin test patterns

It is not possible to switch the input and output modes of bi-directional pins multiple times within one event due to the limits of the tester. Generate test patterns to ensure that the RZ waveform is not used to switch the input and output modes of bi-directional buffers.

A4. I/O Buffer Characteristics

A4.1 5.0V Operation

A4.1.1 Output Current Characteristics (5.0V ±0.5V)

Table A4-1 Output Current Characteristics (5.0V ±0.5V)

	Output current	
Type No.	**I_{OL} (mA)**	**I_{OH} (mA)**
TYPE S	0.1	-0.1
TYPE M	1	-1
TYPE 1	3	-3
TYPE 2	8	-8
TYPE 3	12	-12

"S," "M," and "1" through "3" following "TYPE" are the numbers corresponding to * in the "XX*X" section of the names of output cells.
Example: OB3T indicates TYPE 3.

A4.1.2 Input Buffer Characteristics (5.0V ±0.5V)

- Standard cell input buffer

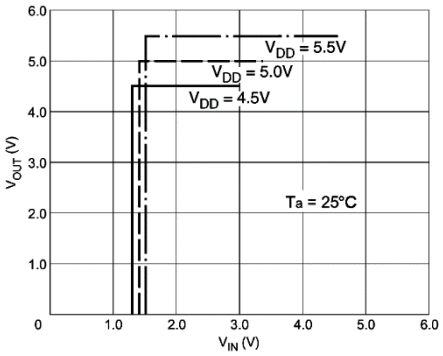


Figure A4-1 Input Characteristic (TTL Level)

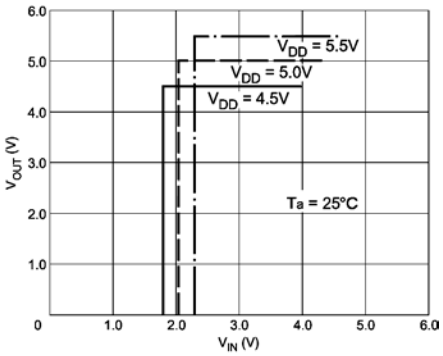


Figure A4-2 Input Characteristic (CMOS Level)

- Schmitt trigger cell input buffer

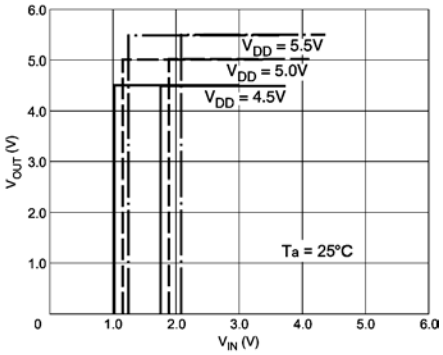


Figure A4-3 Input Characteristic (TTL Level)

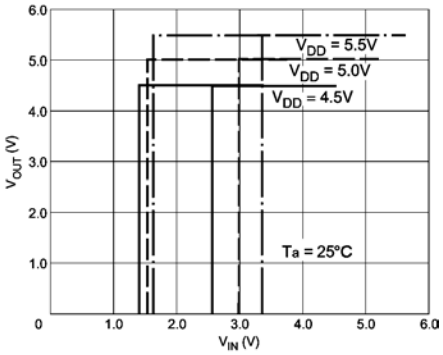


Figure A4-4 Input Characteristic (CMOS Level)

A4.1.3 Output Driver Characteristics

- Low-level output current

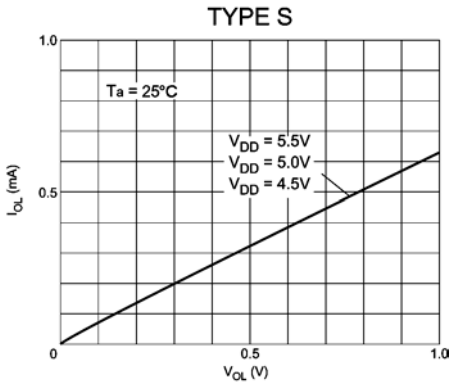


Figure A4-5

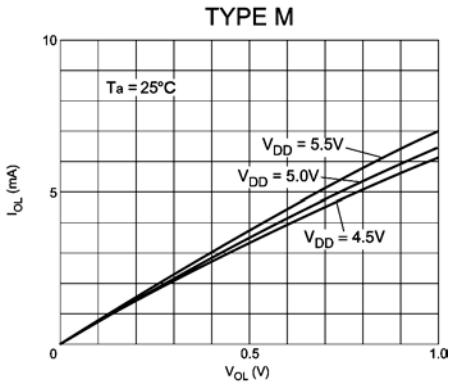


Figure A4-6

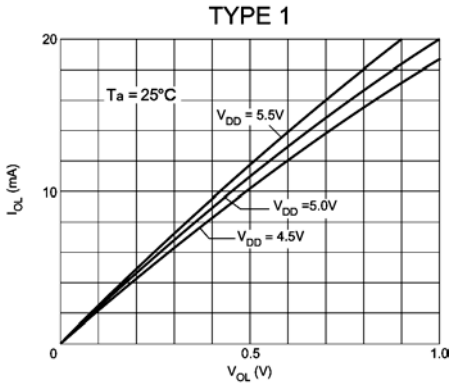


Figure A4-7

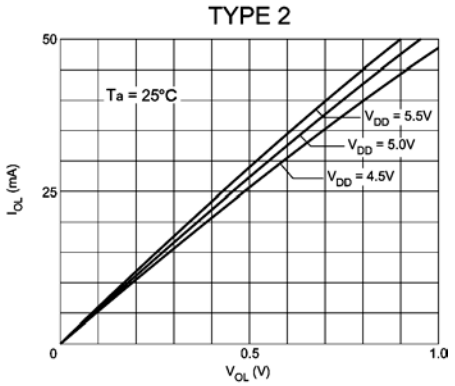


Figure A4-8

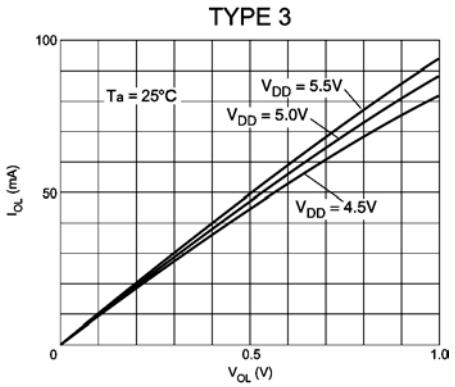


Figure A4-9

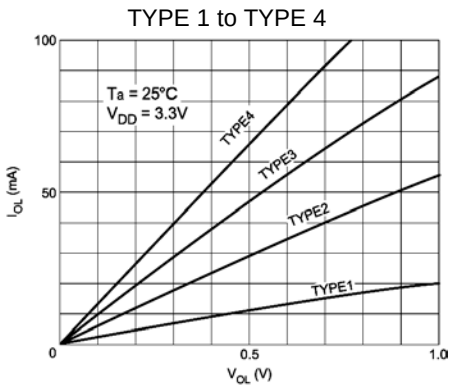


Figure A4-10

- High level output current

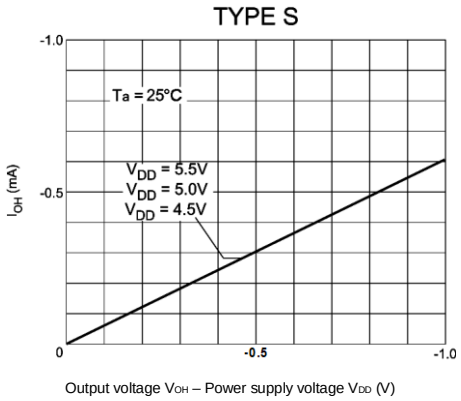


Figure A4-11

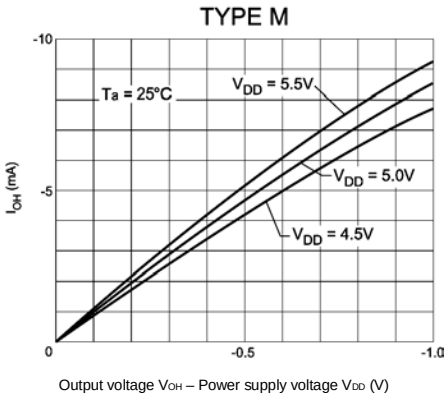


Figure A4-12

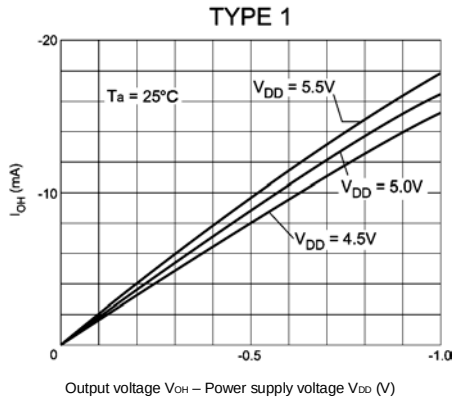


Figure A4-13

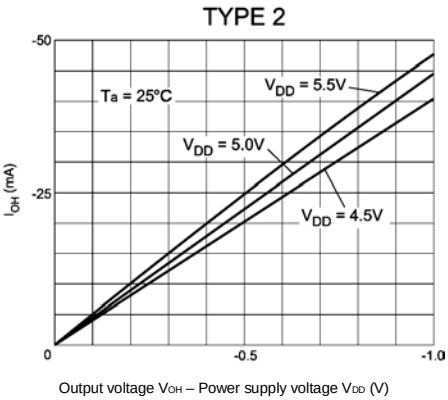


Figure A4-14

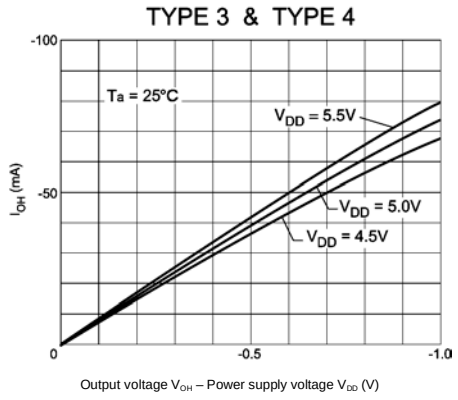


Figure A4-15

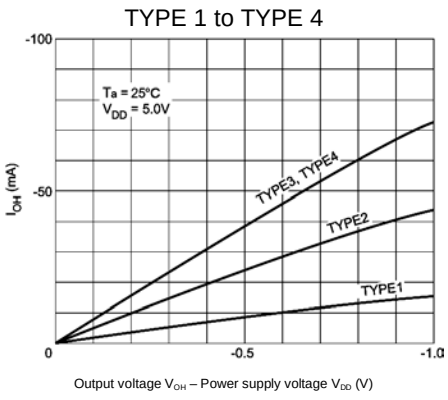


Figure A4-16

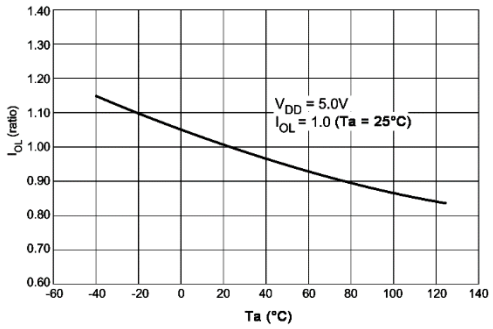


Figure A4-17 Ambient Temperature (Ta) vs. Output Current (I_{OL})

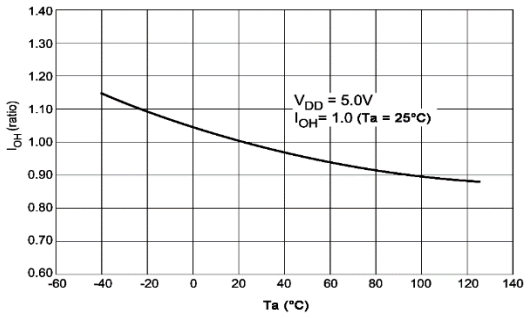


Figure A4-18 Ambient Temperature (Ta) vs. Output Current (I_{OH})

A4.1.4 Output Delay Time vs. Output Load Capacitance (C_L)

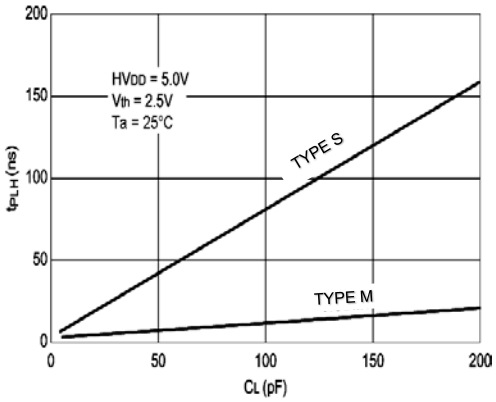


Figure A4-19 Output Delay Tme (t_{PLH}) vs. Output Load Capacitance (C_L)

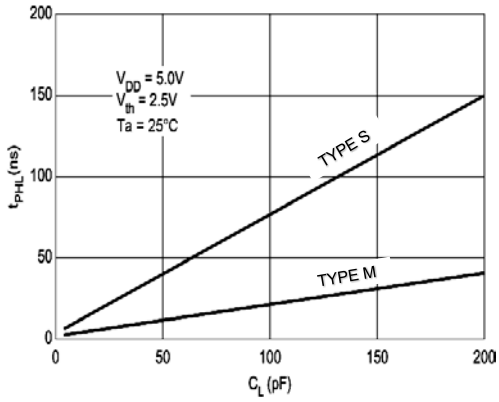


Figure A4-20 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

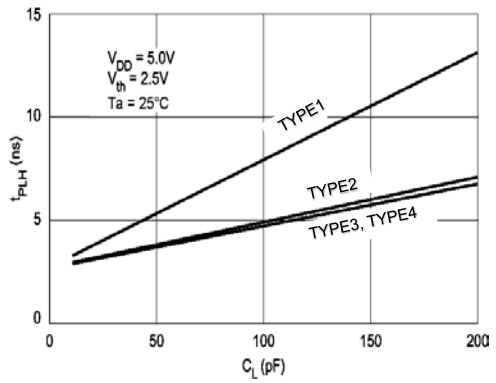


Figure A4-21 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

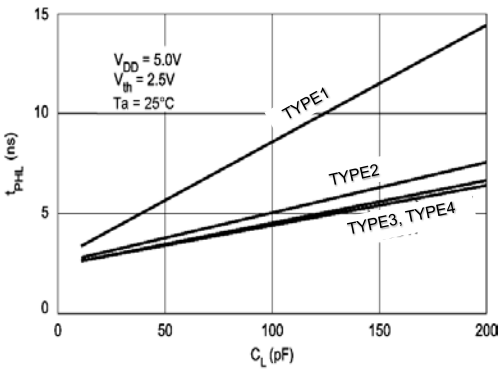


Figure A4-22 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

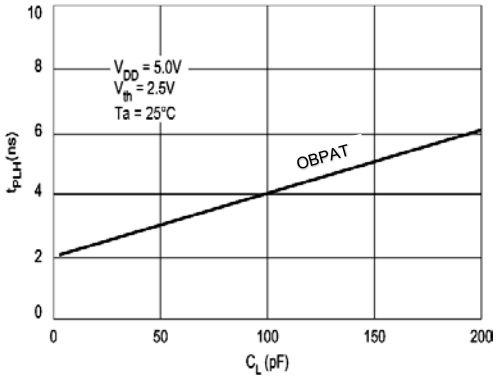


Figure A4-23 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

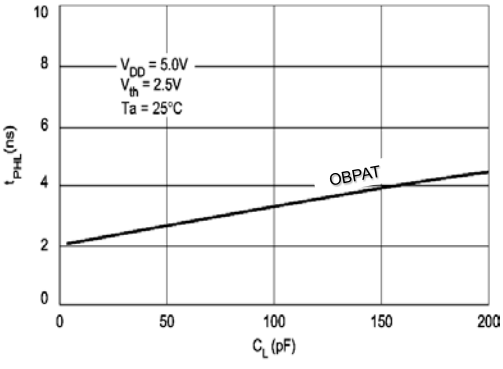


Figure A4-24 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

A4.1.5 Output Buffer Rising/Falling Time vs. Output Load Capacitance (C_L)

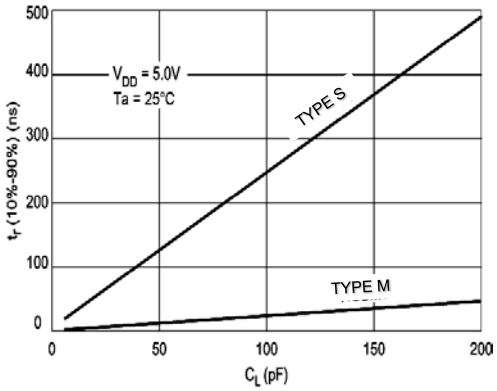


Figure A4-25 Rising Time (t_r) vs. Output Load Capacitance (C_L)

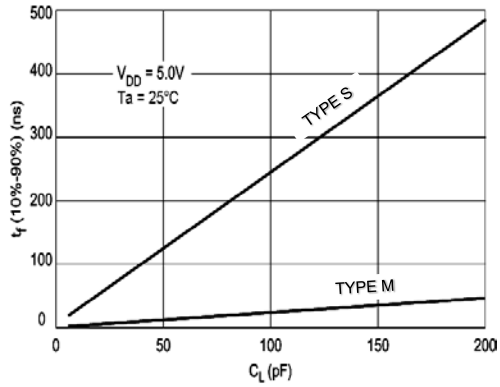


Figure A4-26 Falling Time (t_f) vs. Output Load Capacitance (C_L)

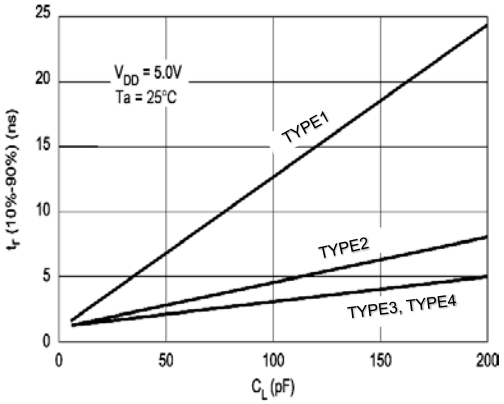


Figure A4-27 Rising Time (t_r) vs. Output Load Capacitance (C_L)

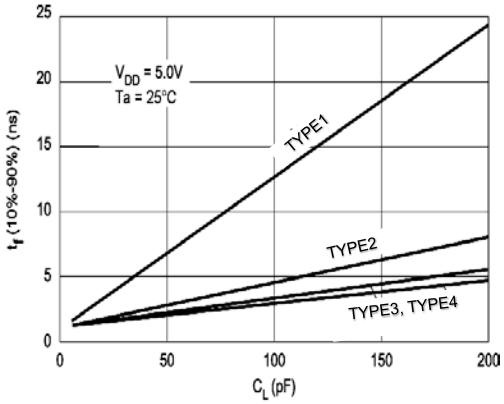


Figure A4-28 Falling Time (t_f) vs. Output Load Capacitance (C_L)

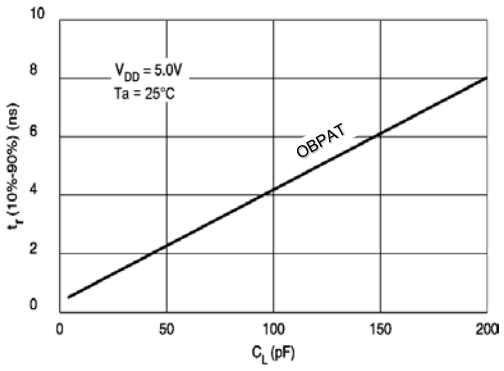


Figure A4-29 Rising Time (t_r) vs. Output Load Capacitance (C_L)

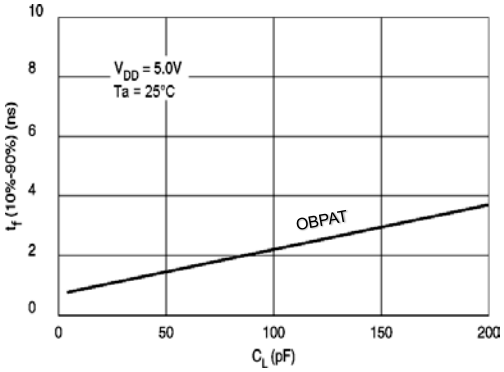


Figure A4-30 Falling Time (t_f) vs. Output Load Capacitance (C_L)

A4.1.6 Pull-up/Pull-down Resistance

- Pull-up characteristics

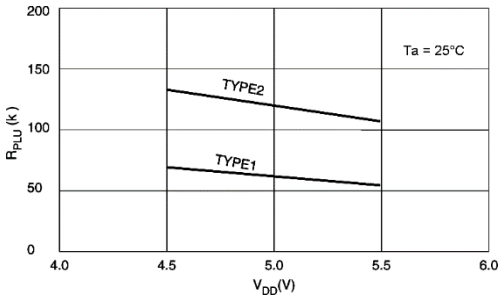


Figure A4-31 Power Supply Voltage Dependency of Pull-up Resistance

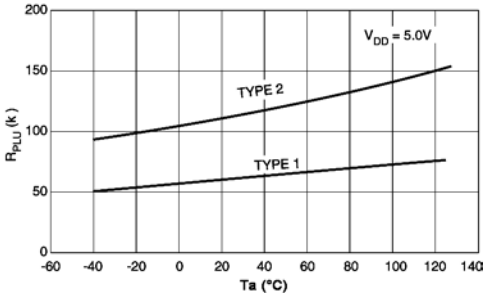


Figure A4-32 Ambient Temperature Dependency of Pull-up Resistance

- Pull-down characteristics

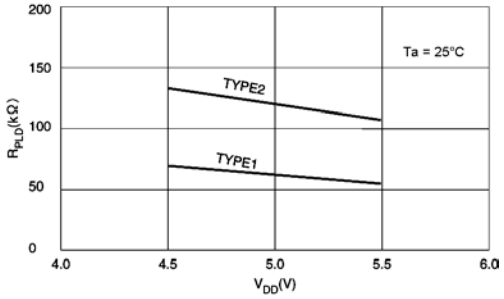


Figure A4-33 Power Supply Voltage Dependency of Pull-down Resistance

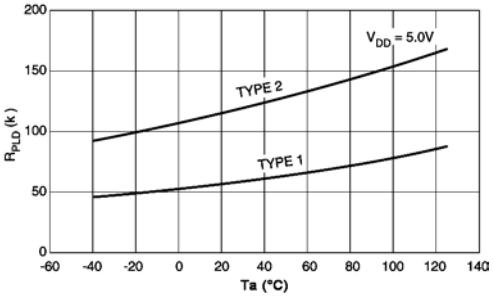


Figure A4-34 Ambient Temperature Dependency of Pull-down Resistance

A4.1.7 Output Waveforms

- High-speed type output buffer waveform (OB3AT)

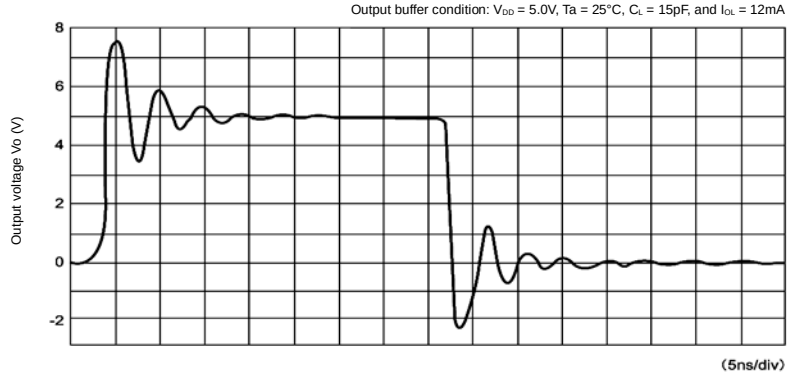


Figure A4-35

- Normal type output buffer waveform (OB3T)

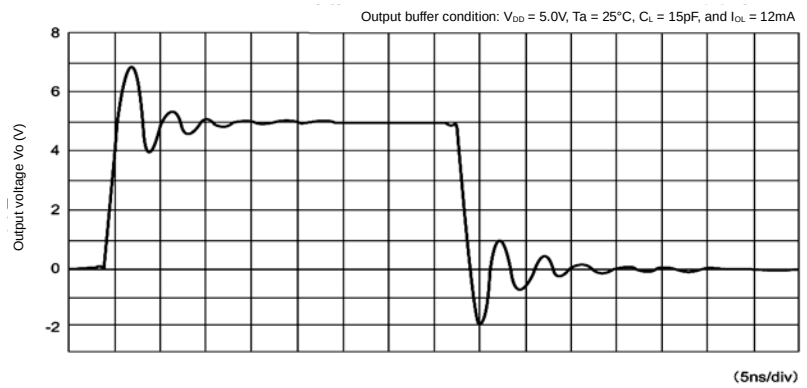


Figure A4-36

- Low-noise type output buffer waveform (OB3BT)

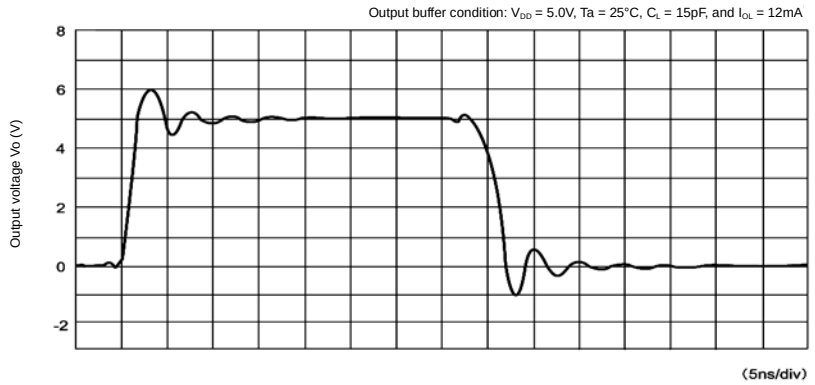


Figure A4-37

A4.2 3.3-V operation

A4.2.1 Output Current Characteristics (3.3V ±0.3V)

Table A4-2 Output Current Characteristics (3.3V ±0.3V)

	Output current	
Type No.	**I_{OL} (mA)**	**I_{OH} (mA)**
TYPE S	0.1	-0.1
TYPE M	1	-1
TYPE 1	2	-2
TYPE 2	6	-6
TYPE 3	12	-12

"S," "M," and "1" through "4" following "TYPE" are the numbers corresponding to * in the "XX*X" section of the names of output cells.
Example: OB3T indicates TYPE 3.

A4.2.2 Input Buffer Characteristics (3.3V ±0.3V)

- Standard cell input buffer

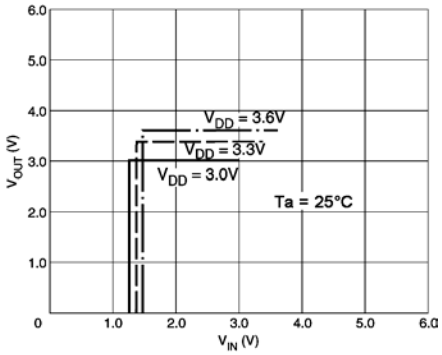


Figure A4-38 Input Characteristic (LVTTL Level)

- Schmitt input buffer

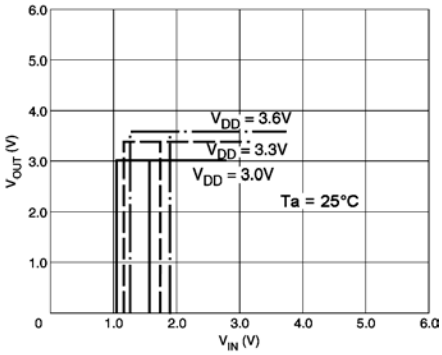


Figure A4-39 Input Characteristic (LVTTL Level)

A4.2.3 Output Driver Characteristics

- Low-level output current

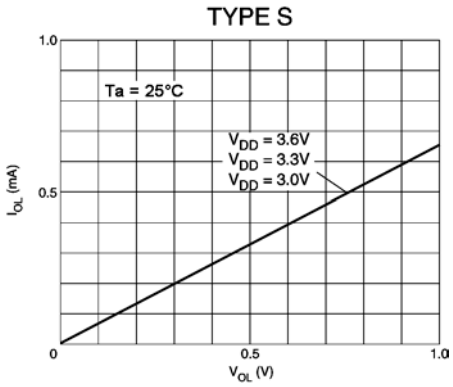


Figure A4-40

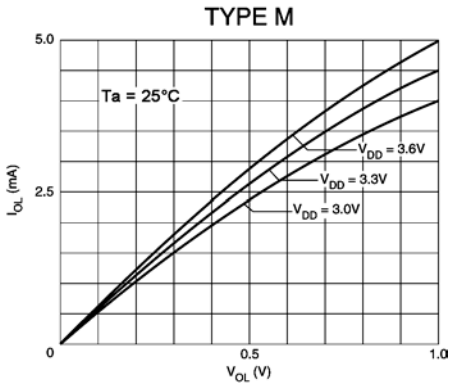


Figure A4-41

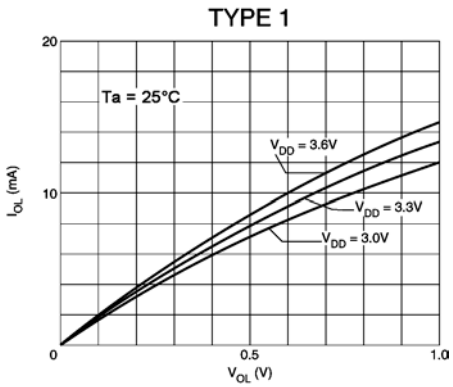


Figure A4-42

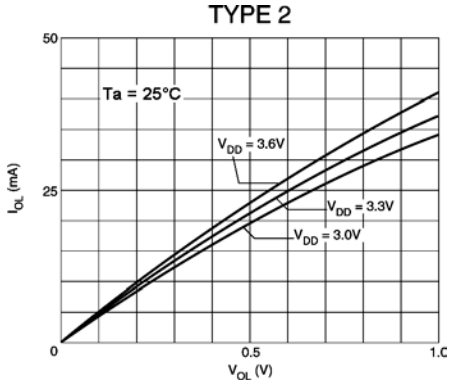


Figure A4-43

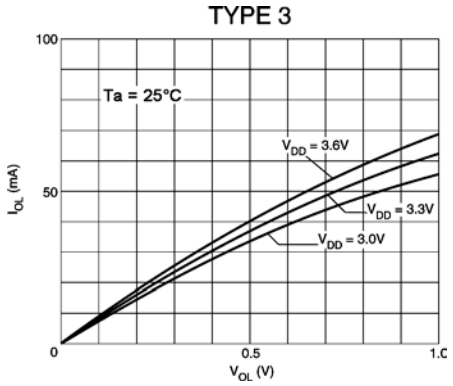


Figure A4-44

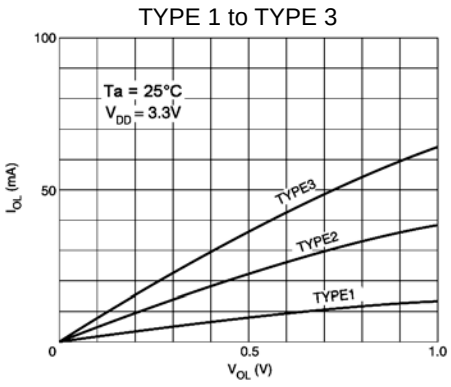


Figure A4-45

- High-level output current

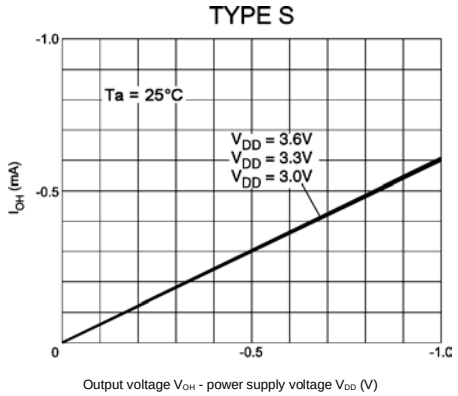


Figure A4-46

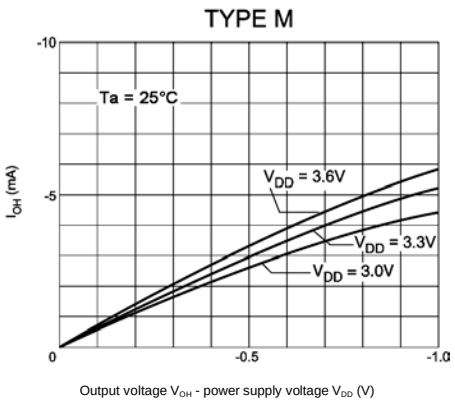


Figure A4-47

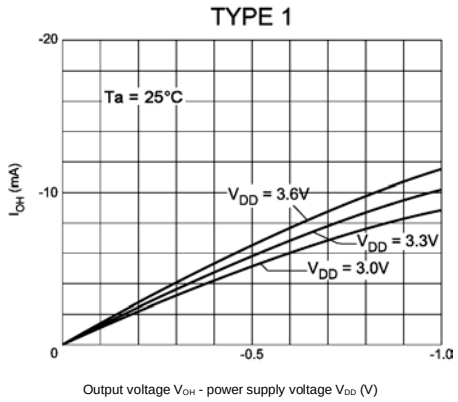


Figure A4-48

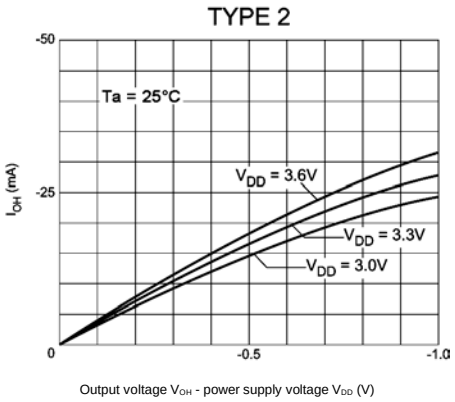


Figure A4-49

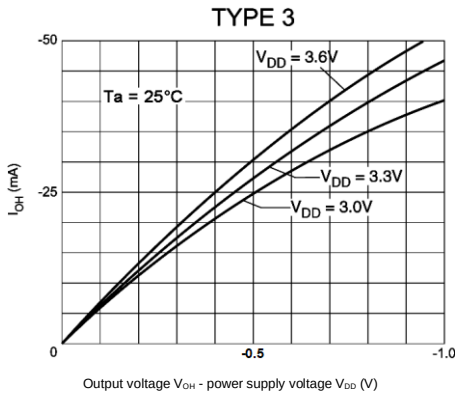


Figure A4-50

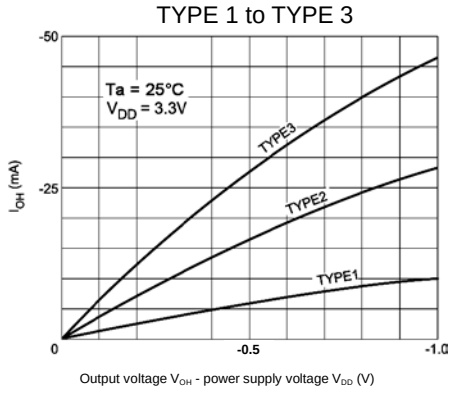
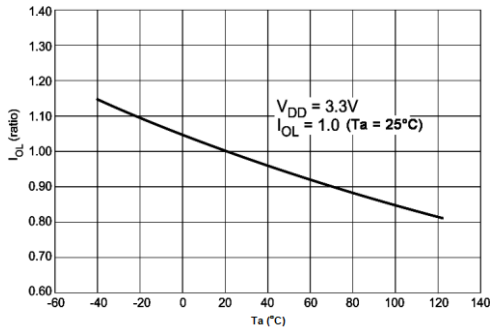
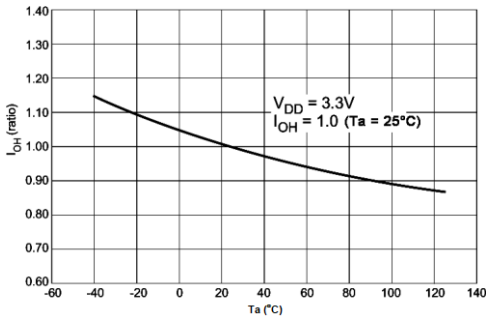


Figure A4-51



Ambient temperature Ta − Output current I_{OL}

Figure A4-52



Ambient temperature Ta − Output current I_{OH}

Figure A4-53

A4.2.4 Output Delay Time vs. Output Load Capacitance (C_L)

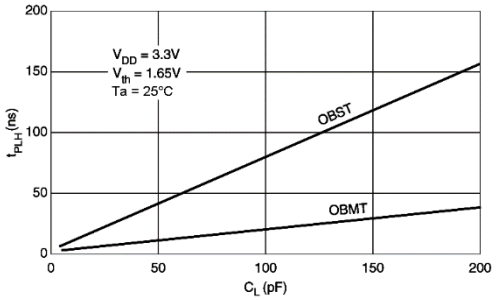


Figure A4-54 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

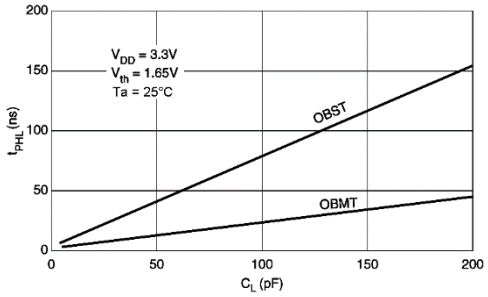


Figure A4-55 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

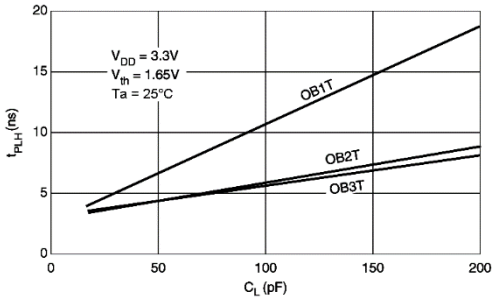


Figure A4-56 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

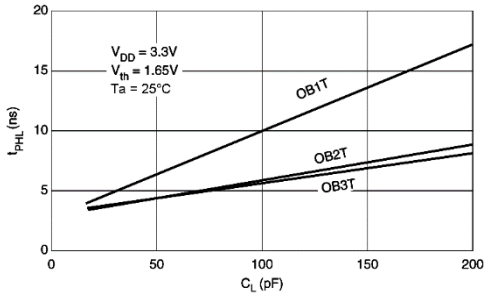


Figure A4-57 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

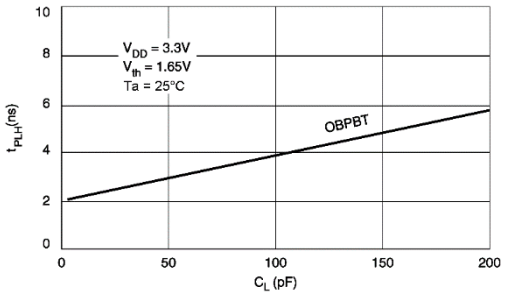


Figure A4-58 Output Delay Time (t_{PLH}) vs. Output Load Capacitance (C_L)

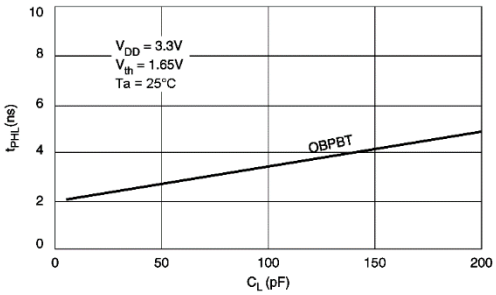


Figure A4-59 Output Delay Time (t_{PHL}) vs. Output Load Capacitance (C_L)

A4.2.5 Output Buffer Rising/Falling Time vs. Output Load Capacitance (C_L)

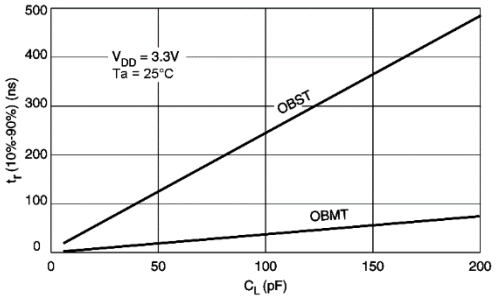


Figure A4-60 Rising Time (t_r) vs. Output Load Capacitance (C_L)

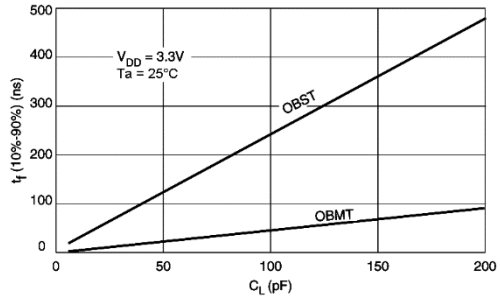


Figure A4-61 Falling Time (t_f) vs. Output Load Capacitance (C_L)

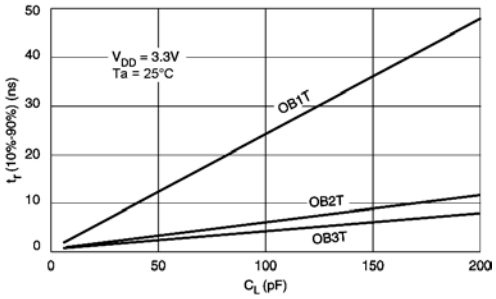


Figure A4-62 Rising Time (t_r) vs. Output Load Capacitance (C_L)

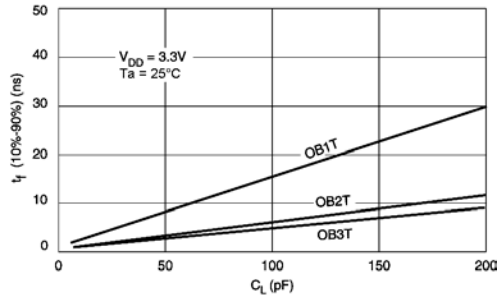


Figure A4-63 Falling Time (t_f) vs. Output Load Capacitance (C_L)

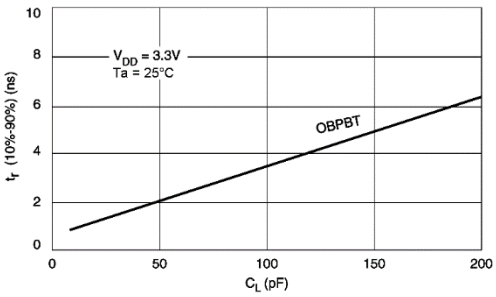


Figure A4-64 Rising Time (t_r) vs. Output Load Capacitance (C_L)

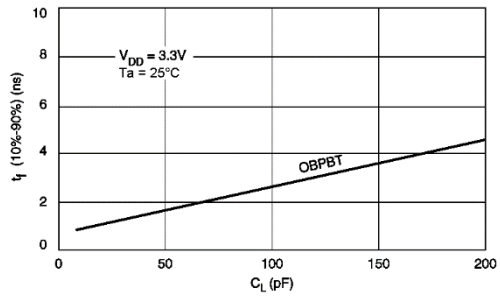


Figure A4-65 Falling Time (t_f) vs. Output Load Capacitance (C_L)

A4.2.6 Pull-up/Pull-down Resistance

- Pull-up characteristics

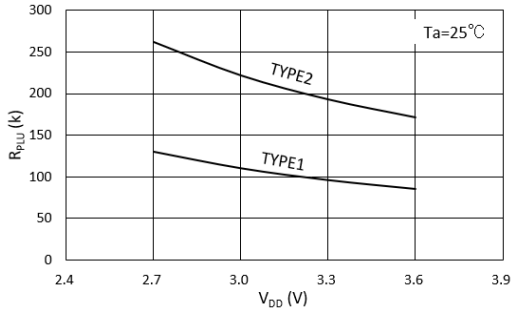


Figure A4-66 Power Supply Voltage Dependency of Pull-up Resistance

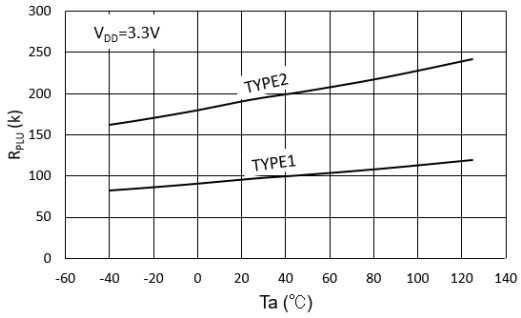


Figure A4-67 Ambient Temperature Dependency of Pull-up Resistance

- Pull-down characteristics

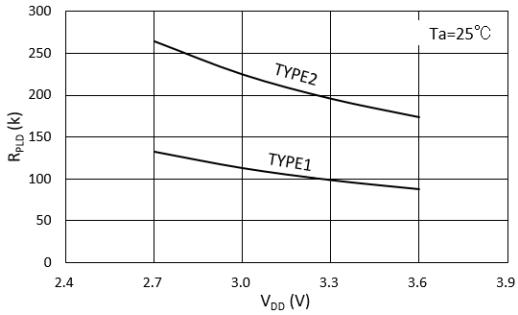


Figure A4-68 Power Supply Voltage Dependency of Pull-down Resistance

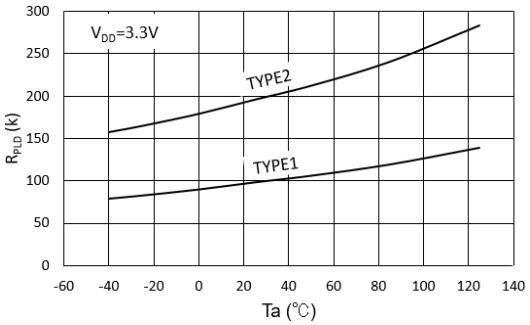


Figure A4-69 Ambient Temperature Dependency of Pull-down Resistance

A4.2.7 Output Waveforms

- High-speed type output buffer waveform (OB3AT)

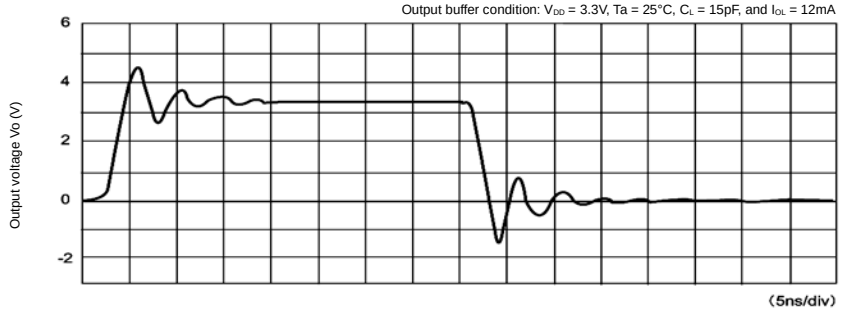


Figure A4-70

- Normal type output buffer waveform (OB3T)

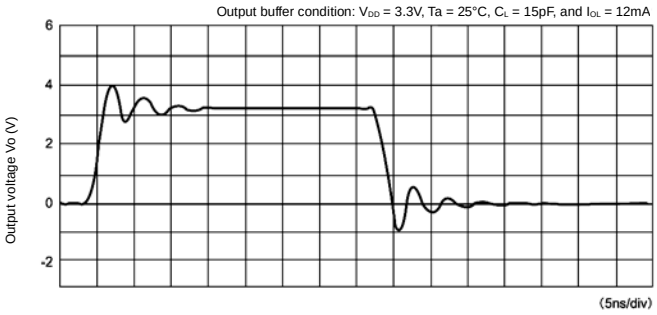


Figure A4-71

- Low-noise type output buffer waveform (OB3BT)

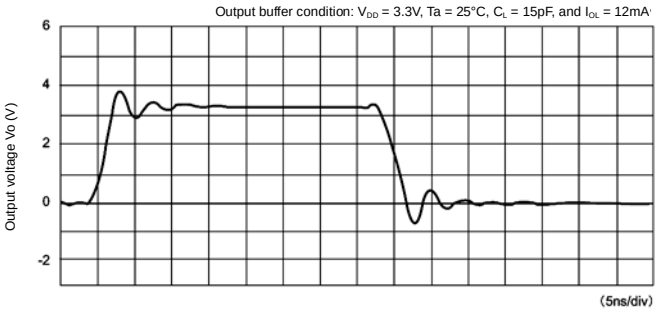


Figure A4-72

A4.3 Schmitt Input Buffer Electrical Characteristics

Figure A4-73 shows the electrical characteristics of Schmitt input buffers. VT+ and VT− are within the respective maximum and minimum specifications and vary depending on individual and environmental conditions. The difference between the two is more than the minimum value for VH.

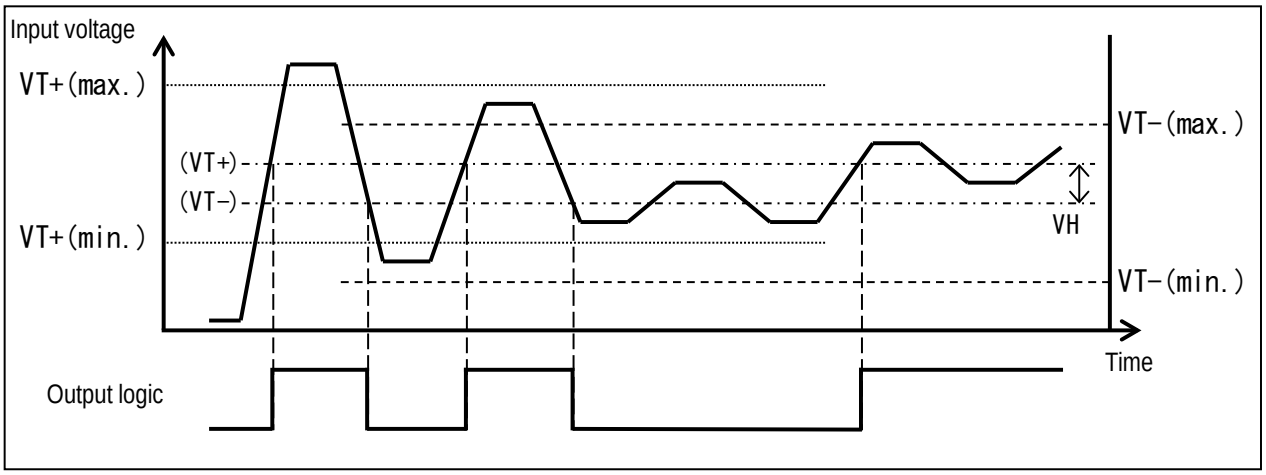


Figure A4-73 Correlation Between Input Voltage and Logic Values for Schmitt Input Buffers

VT+: Voltage at which High is detected when the input signal changes from Low to High

VT−: Voltage at which Low is detected when the input signal changes from High to Low

VH: Voltage difference required to detect the time point when a signal previously detected as High (or Low) changes to Low (or High)

Revision History

Attachment-1

Rev. No.	Year/Month	Page	Category	Revision Details (incl. previous details) and Reason for Revision
Rev. 1.2	2013/7	All pages	New	Issue limited to electrical characteristics
Rev. 1.3	2014/5	All pages	Revision	Complete revision with expansion of information
Rev. 1.4	2015/4	All pages	Revision	Complete revision to make the content consistent with S1X50000/S1L50000 Series revisions
Rev. 1.5	2015/12	All pages	Revision	Addition of Chapter 9 PLL
Rev. 1.6	2016/4	Appendix	Revision	Addition of VHDL to A2 Notes on RTL Design Correction of A3.1 Scan Correction of errors in A5.1.4 and A5.1.5
Rev. 1.7	2016/10	Chapter 5	Revision	Deletion of Figure 5-1 Continuous Oscillation Type and Figure 5-2 Intermittent Oscillation Type in Section 5.1.1
Rev. 1.8	2017/7	Chapters 1 and 8	Revision	Addition of S1L5V48* to Table 1-1-1 S1L5V000 Series Master List in Section 1.2.1 Addition of S1L5V48* to Table 1-7 Static Current Consumption in Section 1.4 Addition of 8.3 Asynchronous RAM Delay Parameters and 8.6 Synchronous RAM Delay Parameters
Rev. 1.9	2018/3	Chapter 1	Revision	Deletion of “under development” for S1L5V48* following official release Addition of A5.3 Schmitt Input Buffer Electrical Characteristics
Rev. 2.0	2019/4	Appendix	Revision	Addition of 3.3V pull-up and pull-down electrical characteristics and temperature characteristics graphs in A5.2.6.
Rev. 3.0	2020/7	All pages	Revision	Overall reorganization
Rev. 3.1	2021/3	P.111	Revision	Change description of 10.2 Limit on power consumption

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