S1C17 Family Technical Manual Errata

ITEM	LCD drive voltage		
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(Error)

Unless otherwise specified: V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta = 25°C, C_1–C_{11} = 0.1μF, Checker pattern displayed, No panel load

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1}		0.18V_{C5}		0.22V_{C5}	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2}		0.39V_{C5}		0.43V_{C5}	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3}		0.59V_{C5}		0.63V_{C5}	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4}		0.79V_{C5}		0.83V_{C5}	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5}	LC[3:0] = 0x0		4.20		V
			LC[3:0] = 0x1		4.30		V
			LC[3:0] = 0x2		4.40		V

(Correct)

Unless otherwise specified: V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta = 25°C, C_1–C_{11} = 0.1μF, Checker pattern displayed, No panel load

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between ~~V_{SS} and V_{C1}~~ V_{C5} and V_{C1}		0.18V_{C5}		0.22V_{C5}	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2}		0.39V_{C5}		0.43V_{C5}	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3}		0.59V_{C5}		0.63V_{C5}	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4}		0.79V_{C5}		0.83V_{C5}	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5}	LC[3:0] = 0x0		4.20		V
			LC[3:0] = 0x1		4.30		V
			LC[3:0] = 0x2		4.40		V

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(Error)

D3　CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.

(Correct)

D3　CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare

A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (CLKEN = 0) before setting CBUFEN.

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(Error)

D3   CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated. When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.

(Correct)

D3   CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated. When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (CLKEN = 0) before setting CBUFEN.

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ITEM Transmission buffer empty interrupt at SPI slave mode			
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		19.7 Control Register Details	15-8

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(Error)

Transmit buffer empty interrupt

To use this interrupt, set SPTIE (D4/SPI_CTL register) to 1. If SPTIE is set to 0 (default), interrupt requests for this factor will not be sent to the ITC.

 * **SPTIE**: Transmit Data Buffer Empty Interrupt Enable Bit in the SPI Control (SPI_CTL) Register
   (D4/0x4326)

When transmission data written to the transmit data buffer is transferred to the shift register, the SPI module sets the SPTBE bit (D0/SPI_ST register) to 1, indicating that the transmit data buffer is empty. If transmit buffer empty interrupts are permitted (SPTIE = 1), an interrupt request pulse is sent simultaneously to the ITC.

 * **SPTBE**: Transmit Data Buffer Empty Flag in the SPI Status (SPI_ST) Register (D0/0x4320)

An interrupt occurs if other interrupt conditions are met.

You can inspect the SPTBE flag in the SPI interrupt processing routine to determine whether the SPI interrupt is attributable to a transmit buffer empty. If SPTBE is 1, the next transmission data can be written to the transmit data buffer by the interrupt processing routine.

(Correct)

Transmit buffer empty interrupt

To use this interrupt, set SPTIE (D4/SPI_CTL register) to 1. If SPTIE is set to 0 (default), interrupt requests for this factor will not be sent to the ITC.

 * **SPTIE**: Transmit Data Buffer Empty Interrupt Enable Bit in the SPI Control (SPI_CTL) Register
   (D4/0x4326)

When transmission data written to the transmit data buffer is transferred to the shift register, the SPI module sets the SPTBE bit (D0/SPI_ST register) to 1, indicating that the transmit data buffer is empty. If transmit buffer empty interrupts are permitted (SPTIE = 1), an interrupt request pulse is sent

simultaneously to the ITC.

* **SPTBE**: Transmit Data Buffer Empty Flag in the SPI Status (SPI_ST) Register (D0/0x4320)

An interrupt occurs if other interrupt conditions are met.

You can inspect the SPTBE flag in the SPI interrupt processing routine to determine whether the SPI interrupt is attributable to a transmit buffer empty. If SPTBE is 1, the next transmission data can be written to the transmit data buffer by the interrupt processing routine.

Note: the transmit buffer empty interrupt can only be used in master mode.

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(Error)

D4 SPTIE: Transmit Data Buffer Empty Interrupt Enable Bit

Permits or prohibits transmit data buffer empty SPI interrupts.

1 (R/W): Permitted

0 (R/W): Prohibited (default)

Setting SPTIE to 1 permits the output of SPI interrupt requests to the ITC due to a transmit data buffer empty. These interrupt requests are generated when the data written to the transmit data buffer is transferred to the shift register (when transmission starts). SPI interrupts are not generated by transmit data buffer empty if SPTIE is set to 0.

(Correct)

D4 SPTIE: Transmit Data Buffer Empty Interrupt Enable Bit

Permits or prohibits transmit data buffer empty SPI interrupts.

1 (R/W): Permitted

0 (R/W): Prohibited (default)

Setting SPTIE to 1 permits the output of SPI interrupt requests to the ITC due to a transmit data buffer empty. These interrupt requests are generated when the data written to the transmit data buffer is transferred to the shift register (when transmission starts). SPI interrupts are not generated by transmit data buffer empty if SPTIE is set to 0.

Note: the transmit buffer empty interrupt can only be used in master mode.

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(Error)

• Do not access the SPI_CTL register (0x4326) while the SPBY flag (D2/SPI_ST register) is set to 1, or the SPRBF flag (D1/SPI_ST register) is set to 1 (while sending or receiving data).

* **SPBSY**: Transfer Busy Flag in the SPI Status (SPI_ST) Register (D2/0x4320)

* **SPRBF**: Receive Data Buffer Full Flag in the SPI Status (SPI_ST) Register (D1/0x4320)

• Do not gain write access to read registers (the SPI_ST and SPI_RXD registers) while sending/receiving data via SPI.

(Correct)

• Do not access the SPI_CTL register (0x4326) while the SPBY flag (D2/SPI_ST register) is set to 1, or the SPRBF flag (D1/SPI_ST register) is set to 1 (while sending or receiving data).

   * **SPBSY**: Transfer Busy Flag in the SPI Status (SPI_ST) Register (D2/0x4320)

   * **SPRBF**: Receive Data Buffer Full Flag in the SPI Status (SPI_ST) Register (D1/0x4320)

• Do not gain write access to read registers (the SPI_ST and SPI_RXD registers) while sending/receiving data via SPI.

• The transmit buffer empty interrupt can only be used in master mode.

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(Error)

Transmit buffer empty interrupt

To use this interrupt, set SPTIE/SPI_CTLx register to 1. If SPTIE is set to 0 (default), interrupt requests for this factor will not be sent to the ITC.

When transmission data written to the transmit data buffer is transferred to the shift register, the SPI module sets the SPTBE/SPI_STx register to 1, indicating that the transmit data buffer is empty. If transmit buffer empty interrupts are permitted (SPTIE = 1), an interrupt request pulse is sent simultaneously to the ITC.

An interrupt occurs if other interrupt conditions are met. You can inspect the SPTBE flag in the SPI interrupt handler routine to determine whether the SPI interrupt is attributable to a transmit buffer empty. If SPTBE is 1, the next transmit data can be written to the transmit data buffer by the interrupt handler routine.

(Correct)

Transmit buffer empty interrupt

To use this interrupt, set SPTIE/SPI_CTLx register to 1. If SPTIE is set to 0 (default), interrupt requests for this factor will not be sent to the ITC.

When transmission data written to the transmit data buffer is transferred to the shift register, the SPI module sets the SPTBE/SPI_STx register to 1, indicating that the transmit data buffer is empty. If transmit buffer empty interrupts are permitted (SPTIE = 1), an interrupt request pulse is sent simultaneously to the ITC.

An interrupt occurs if other interrupt conditions are met. You can inspect the SPTBE flag in the SPI interrupt handler routine to determine whether the SPI interrupt is attributable to a transmit buffer empty. If SPTBE is 1, the next transmit data can be written to the transmit data buffer by the interrupt handler routine.

Note: the transmit buffer empty interrupt can only be used in master mode.

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(Error)

D4 SPTIE: Transmit Data Buffer Empty Interrupt Enable Bit

Enables or disables SPI transmit data buffer empty interrupts.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting SPTIE to 1 enables the output of SPI interrupt requests to the ITC due to a transmit data buffer empty. These interrupt requests are generated when the data written to the transmit data buffer is transferred to the shift register (when transmission starts).

SPI interrupts are not generated by transmit data buffer empty if SPTIE is set to 0.

(Correct)

D4 SPTIE: Transmit Data Buffer Empty Interrupt Enable Bit

Enables or disables SPI transmit data buffer empty interrupts.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting SPTIE to 1 enables the output of SPI interrupt requests to the ITC due to a transmit data buffer empty. These interrupt requests are generated when the data written to the transmit data buffer is transferred to the shift register (when transmission starts).

SPI interrupts are not generated by transmit data buffer empty if SPTIE is set to 0.

Note: the transmit buffer empty interrupt can only be used in master mode.