Dec/10/2020

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ITEM: Appendix D Measures Against Noise			
Object manuals	Document codes	Items	Pages
S1C17M20/M21/M22/M23/ M24/M25 Technical Manual	413557000	Appendix D Measures Against Noise	AP-D-1
S1C17M40 Technical Manual	413895200	Appendix D Measures Against Noise	AP-D-1
S1C17F63 Technical Manual	413942900	Appendix D Measures Against Noise	AP-D-1

（Error）

No description

（Correct）

Noise Measures for input terminals connected to signals with high drive capability such as power supplies

If there are terminals that are directly connected to the output of a power supply or a device with high drive capability, a large current may flow due to noise entering these terminals. In such a case insert a resistor of 30Ω or more in series to protect the terminals. Determine the resistance value after evaluation on the mounting board. When connecting the power supply directly to the VREFA terminal, insert a 100Ω resistor in series. In this case, there is no effect on the characteristics of the ADC.

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ITEM: Corrective operation when a value out of the effective range is set			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	8.4.2 Real-Time Clock Counter Operations	8-4
S1C17M10Technical Manual	413180200	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17M20/M21/M22/M23/M24/M25Technical Manual	413557000	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17M30/M31/M32/M33/M34Technical Manual	413495601	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17M40Technical Manual	413895200	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W03/W04Technical Manual	412925001	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W12/13Technical Manual	413520201	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W14/W16Technical Manual	412910300	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W15Technical Manual	412645702	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W18Technical Manual	413129601	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W22/W23Technical Manual	412690402	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W34/W35/W36Technical Manual	413237901	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17F63Technical Manual	413942900	21.4.2Real-Time Clock Function	21-6

(Error)

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing.

(Correct)

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing of the counter. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing of the counter.

Note: RTCMON.RTCMOH bits=0 & RTCMON.RTCMOL[3:0] bits=0x0 are prohibited.

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errata_c17m20-21-22-23-24-25_7

S1C17 Manual errata

ITEM: Real-Time Clock (RTCA) Theoretical Regulation Function			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	8.3.2 Theoretical Regulation Function	8-2
S1C17M10Technical Manual	413180200	9.3.2 Theoretical Regulation Function	9-2
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	9.3.2 Theoretical Regulation Function	9-2
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	9.3.2 Theoretical Regulation Function	9-2
S1C17W03/W04Technical Manual	412925001	9.3.2 Theoretical Regulation Function	9-2
S1C17W12/W13Technical Manual	413520201	9.3.2 Theoretical Regulation Function	9-2
S1C17W14/W16Technical Manual	412910200	9.3.2 Theoretical Regulation Function	9-2
S1C17W15Technical Manual	412645602	9.3.2 Theoretical Regulation Function	9-2
S1C17W18Technical Manual	413129501	9.3.2 Theoretical Regulation Function	9-2
S1C17W22/W23Technical Manual	412690302	9.3.2 Theoretical Regulation Function	9-2
S1C17W34/W35/W36Technical Manual	413237401	9.3.2 Theoretical Regulation Function	9-2

(Error)

9.3.2 Theoretical Regulation Function

The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.

1. Measure the frequency tolerance “m [ppm]” of f_{OSC1}.
2. Determine the theoretical regulation execution cycle time “n seconds.”
3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2.
4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt.
5. Monitor the RTC1S signal to check that every n-second cycle has no error included.

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two’s-complement number. Use Eq. 9.1 to calculate the correction value.

n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.
RTCTRM[6:0] bits periodically via software)
m: OSC1 frequency tolerance [ppm]

(Correct)

9.3.2 Theoretical Regulation Function

The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.

1. Determine the correction value of frequency tolerance "m [ppm] =- {(f_{OSC1}-32768[Hz]) / 32768[Hz]}×10^6" by measuring the f_{OSC1}.
2. Determine the theoretical regulation execution cycle time "n seconds."
3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2.
4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt.
5. Monitor the RTC1S signal to check that every n-second cycle has no error included.

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two's-complement number. Use Eq. 9.1 to calculate the correction value.

n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.
RTCTRM[6:0] bits periodically via software)
m: OSC1's correction value of frequency tolerance [ppm]

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errata_c17m20-21-22-23-24-25_06

S1C17 Manual errata

ITEM: Reset hold circuit characteristics			
Object manuals	Document codes	Items	Pages
S1C17M10Technical Manual	413180200	19.4 System Reset Controller (SRC) Characteristics	19-3
S1C17M20/M21/M22/M23/M24 /M25 Technical Manual	413557000	21.4 System Reset Controller (SRC) Characteristics	21-4
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	23.4 System Reset Controller (SRC) Characteristics	23-4
S1C17W03/W04Technical Manual	412925001	21.4 System Reset Controller (SRC) Characteristics	21-4
S1C17W12/W13Technical Manual	413520201	21.4 System Reset Controller (SRC) Characteristics	21-4
S1C17W14/W16Technical Manual	412910200	22.4 System Reset Controller (SRC) Characteristics	22-4
S1C17W15Technical Manual	412645602	20.4 System Reset Controller (SRC) Characteristics	20-4
S1C17W18Technical Manual	413129501	23.4 System Reset Controller (SRC) Characteristics	23-4
S1C17W22/W23Technical Manual	412690302	23.4 System Reset Controller (SRC) Characteristics	23-4
S1C17W34/W35/W36Technical Manual	413237401	23.4 System Reset Controller (SRC) Characteristics	23-4
S7C17M11Technical Manual	413393900	21.4 System Reset Controller (SRC) Characteristics	21-4

S1C17M10/M20/M21/M22/M23/M24/M25/M30/M31/M32/M33/M34/S7C17M11

(Error)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		-	-	200	uS

(Correct)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		0.5	-	0.9	mS

S1C17W03/W04/W12/W13/W15/W14/W16/W18/W22/W23/W34/W35/W36

(Error)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		-	-	1.7	mS

(Correct)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		0.5	-	0.9	mS

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errata_c17m20-21-22-23-24-25_05

S1C17 Manual errata

ITEM: Absolute Maximum Ratings of #RESET pin

Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	17.1 Absolute Maximum Ratings	17-1
S1C17M10Technical Manual	413180200	19.1 Absolute Maximum Ratings	19-1
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	21.1 Absolute Maximum Ratings	21-1
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	23.1 Absolute Maximum Ratings	23-1
S1C17W03/W04Technical Manual	412925001	21.1 Absolute Maximum Ratings	21-1
S1C17W12/W13Technical Manual	413520201	21.1 Absolute Maximum Ratings	21-1
S1C17W14/W16Technical Manual	412910200	22.1 Absolute Maximum Ratings	22-1
S1C17W15Technical Manual	412645602	20.1 Absolute Maximum Ratings	20-1
S1C17W18Technical Manual	413129501	23.1Absolute Maximum Ratings	23-1
S1C17W22/W23Technical Manual	412690302	23.1Absolute Maximum Ratings	23-1
S1C17W34/W35/W36Technical Manual	413237401	23.1Absolute Maximum Ratings	23-1
S7C17M11Technical Manual	413393900	21.1Absolute Maximum Ratings	21-1

(Error)

Item	Symbol	Condition	Rated value	Unit
Input voltage	V_I	Pxx	-0.3~7.0	V
		Pyy	-0.3~V_{DD}+0.5	V

(Correct)

Item	Symbol	Condition	Rated value	Unit
Input voltage	V_I	Pxx	-0.3~7.0	V
		Pyy, #RESET	-0.3~V_{DD}+0.5	V

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S1C17 Manual errata

ITEM: Debugger Prohibition of pull-down for DSIO pin			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	3.3.3 List of debugger input/output pins	3-3
S1C17M10Technical Manual	413180200	3.3.3 List of debugger input/output pins	3-3
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	3.3.3 List of debugger input/output pins	3-3
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	3.3.3 List of debugger input/output pins	3-3
S1C17W03/W04Technical Manual	412925001	3.3.3 List of debugger input/output pins	3-3
S1C17W12/W13Technical Manual	413520201	3.3.3 List of debugger input/output pins	3-3
S1C17W14/W16Technical Manual	412910200	3.3.3 List of debugger input/output pins	3-3
S1C17W15Technical Manual	412645602	3.3.3 List of debugger input/output pins	3-3
S1C17W18Technical Manual	413129501	3.3.3 List of debugger input/output pins	3-3
S1C17W22/W23Technical Manual	412690302	3.3.3 List of debugger input/output pins	3-3
S1C17W34/W35/W36Technical Manual	413237401	3.3.3 List of debugger input/output pins	3-3
S7C17M11Technical Manual	413393900	3.3.3 List of debugger input/output pins	3-3

(Error)

3.3.3 List of Debugger Input/Output Pins

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the "I/O Ports" chapter.

Note: Do not drive the DCLK pin with a high level from outside (e.g. pulling up with a resistor). Also, do not connect (short-circuit) between the DCLK pin and another GPIO port. In the both cases, the IC may not start up normally due to unstable pin input/output status at power on.

(Correct)

3.3.3 List of Debugger Input/Output Pins

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the "I/O Ports" chapter.

Note:

- Do not drive the DCLK pin with a high level from outside (e.g. pulling up with a resistor). Also, do not connect (short-circuit) between the DCLK pin and another GPIO port. In the both cases, the IC may not start up normally due to unstable pin input/output status at power on.
- Do not drive the DSIO pin with a low level from outside. Then the CPU enters DEBUG mode by a debug interrupt.

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S1C17 Manual errata

ITEM: Real-Time Clock (RTCA) Notice of RTC Month Register			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	8.6 Control Registers	8-6
S1C17M10Technical Manual	413180200	9.6 Control Registers	9-11
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	9.6 Control Registers	9-11
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	9.6 Control Registers	9-11
S1C17W03/W04Technical Manual	412925001	9.6 Control Registers	9-11
S1C17W12/W13Technical Manual	413520201	9.6 Control Registers	9-11
S1C17W14/W16Technical Manual	412910200	9.6 Control Registers	9-11
S1C17W15Technical Manual	412645602	9.6 Control Registers	9-11
S1C17W18Technical Manual	413129501	9.6 Control Registers	9-11
S1C17W22/W23Technical Manual	412690302	9.6 Control Registers	9-11
S1C17W34/W35/W36Technical Manual	413237401	9.6 Control Registers	9-11

(Error)

RTC Month/Day Register

Bit 12 RTCMOH

Bits 11–8 RTCMOL[3:0]

The RTCMON.RTCMOH bit and the RTCMON.RTCMOL[3:0] bits are used to set and read the 10-month digit and the 1-month digit of the month counter, respectively. The setting/read values are a BCD code within the range from 1 to 12.

Note: Be sure to avoid writing to the RTCMON.RTCMOH/RTCMOL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

(Correct)

RTC Month/Day Register

Bit 12 RTCMOH

Bits 11–8 RTCMOL[3:0]

The RTCMON.RTCMOH bit and the RTCMON.RTCMOL[3:0] bits are used to set and read the 10-month digit and the 1-month digit of the month counter, respectively. The setting/read values are a BCD code within the range from 1 to 12.

Note:

- Be sure to avoid writing to the RTCMON.RTCMOH/RTCMOL[3:0] bits while the RTCCTL.RTCBSY bit = 1.
- Be sure to avoid setting 0x00 to the RTCMON.RTCMOH/RTCMOL[3:0] bits.

Oct/02/2018

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S1C17 Manual errata

ITEM: Sound Generator (SNDA) Clock Division Ratio Settings

Object manuals	Document codes	Items	Pages
S1C17M20/M21/M22/M23/M24/ M25 Technical Manual	413557000	16.6 Control Register	16-10
S1C17M30/M31/M32/M33/M34 Technical Manual	413495601	16.6 Control Register	16-10

(Error)

Table 16.6.1 Clock Source and Division Ratio Settings

SNDCLK. CLKDIV[2:0] bits	SNDCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x7	Reserved	1/1	Reserved	1/1
0x6				
0x5	1/128		1/128	
0x4	1/64		1/64	
0x3	1/32		1/32	
0x2	1/16		1/16	
0x1	1/8		1/8	
0x0	1/4		1/4	

(Correct)

Table 16.6.1 Clock Source and Division Ratio Settings

SNDCLK. CLKDIV[2:0] bits	SNDCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x7	Reserved	1/1	Reserved	1/1
0x6				
0x5	1/512		1/512	
0x4	1/256		1/256	
0x3	1/128		1/128	
0x2	1/64		1/64	
0x1	1/32		1/32	
0x0	1/16		1/16	