Dec/10/2020

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S1C17 Manual errata

ITEM: Corrective operation when a value out of the effective range is set			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	8.4.2 Real-Time Clock Counter Operations	8-4
S1C17M10Technical Manual	413180200	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17M20/M21/M22/M23/M24/M25Technical Manual	413557000	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17M30/M31/M32/M33/M34Technical Manual	413495601	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17M40Technical Manual	413895200	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W03/W04Technical Manual	412925001	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W12/13Technical Manual	413520201	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W14/W16Technical Manual	412910300	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W15Technical Manual	412645702	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W18Technical Manual	413129601	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W22/W23Technical Manual	412690402	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W34/W35/W36Technical Manual	413237901	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17F63Technical Manual	413942900	21.4.2Real-Time Clock Function	21-6

(Error)

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing.

(Correct)

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing of the counter. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing of the counter.

Note: RTCMON.RTCMOH bits=0 & RTCMON.RTCMOL[3:0] bits=0x0 are prohibited.

Nov/25/2019

errata_c17w03-04_17

S1C17 Manual errata

ITEM: Real-Time Clock (RTCA) Theoretical Regulation Function			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	8.3.2 Theoretical Regulation Function	8-2
S1C17M10Technical Manual	413180200	9.3.2 Theoretical Regulation Function	9-2
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	9.3.2 Theoretical Regulation Function	9-2
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	9.3.2 Theoretical Regulation Function	9-2
S1C17W03/W04Technical Manual	412925001	9.3.2 Theoretical Regulation Function	9-2
S1C17W12/W13Technical Manual	413520201	9.3.2 Theoretical Regulation Function	9-2
S1C17W14/W16Technical Manual	412910200	9.3.2 Theoretical Regulation Function	9-2
S1C17W15Technical Manual	412645602	9.3.2 Theoretical Regulation Function	9-2
S1C17W18Technical Manual	413129501	9.3.2 Theoretical Regulation Function	9-2
S1C17W22/W23Technical Manual	412690302	9.3.2 Theoretical Regulation Function	9-2
S1C17W34/W35/W36Technical Manual	413237401	9.3.2 Theoretical Regulation Function	9-2

(Error)

9.3.2 Theoretical Regulation Function

The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.

1. Measure the frequency tolerance "m [ppm]" of f_{OSC1}.
2. Determine the theoretical regulation execution cycle time "n seconds."
3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2.
4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt.
5. Monitor the RTC1S signal to check that every n-second cycle has no error included.

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two's-complement number. Use Eq. 9.1 to calculate the correction value.

n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.
RTCTRM[6:0] bits periodically via software)
m: OSC1 frequency tolerance [ppm]

(Correct)

9.3.2 Theoretical Regulation Function

The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.

1. Determine the correction value of frequency tolerance "m [ppm] =- {(f_{OSC1}-32768[Hz]) / 32768[Hz]}×10^6" by measuring the f_{OSC1}.
2. Determine the theoretical regulation execution cycle time "n seconds."
3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2.
4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt.
5. Monitor the RTC1S signal to check that every n-second cycle has no error included.

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two's-complement number. Use Eq. 9.1 to calculate the correction value.

n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.
RTCTRM[6:0] bits periodically via software)
m: OSC1's correction value of frequency tolerance [ppm]

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S1C17 Manual errata

ITEM: Reset hold circuit characteristics			
Object manuals	Document codes	Items	Pages
S1C17M10Technical Manual	413180200	19.4 System Reset Controller (SRC) Characteristics	19-3
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	21.4 System Reset Controller (SRC) Characteristics	21-4
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	23.4 System Reset Controller (SRC) Characteristics	23-4
S1C17W03/W04Technical Manual	412925001	21.4 System Reset Controller (SRC) Characteristics	21-4
S1C17W12/W13Technical Manual	413520201	21.4 System Reset Controller (SRC) Characteristics	21-4
S1C17W14/W16Technical Manual	412910200	22.4 System Reset Controller (SRC) Characteristics	22-4
S1C17W15Technical Manual	412645602	20.4 System Reset Controller (SRC) Characteristics	20-4
S1C17W18Technical Manual	413129501	23.4 System Reset Controller (SRC) Characteristics	23-4
S1C17W22/W23Technical Manual	412690302	23.4 System Reset Controller (SRC) Characteristics	23-4
S1C17W34/W35/W36Technical Manual	413237401	23.4 System Reset Controller (SRC) Characteristics	23-4
S7C17M11Technical Manual	413393900	21.4 System Reset Controller (SRC) Characteristics	21-4

S1C17M10/M20/M21/M22/M23/M24/M25/M30/M31/M32/M33/M34/S7C17M11

(Error)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		-	-	200	uS

(Correct)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		0.5	-	0.9	mS

S1C17W03/W04/W12/W13/W15/W14/W16/W18/W22/W23/W34/W35/W36

(Error)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		-	-	1.7	mS

(Correct)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		0.5	-	0.9	mS

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S1C17 Manual errata

ITEM: Absolute Maximum Ratings of #RESET pin

Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	17.1 Absolute Maximum Ratings	17-1
S1C17M10Technical Manual	413180200	19.1 Absolute Maximum Ratings	19-1
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	21.1 Absolute Maximum Ratings	21-1
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	23.1 Absolute Maximum Ratings	23-1
S1C17W03/W04Technical Manual	412925001	21.1 Absolute Maximum Ratings	21-1
S1C17W12/W13Technical Manual	413520201	21.1 Absolute Maximum Ratings	21-1
S1C17W14/W16Technical Manual	412910200	22.1 Absolute Maximum Ratings	22-1
S1C17W15Technical Manual	412645602	20.1 Absolute Maximum Ratings	20-1
S1C17W18Technical Manual	413129501	23.1Absolute Maximum Ratings	23-1
S1C17W22/W23Technical Manual	412690302	23.1Absolute Maximum Ratings	23-1
S1C17W34/W35/W36Technical Manual	413237401	23.1Absolute Maximum Ratings	23-1
S7C17M11Technical Manual	413393900	21.1Absolute Maximum Ratings	21-1

(Error)

Item	Symbol	Condition	Rated value	Unit
Input voltage	V_I	Pxx	-0.3~7.0	V
		Pyy	-0.3~V_{DD}+0.5	V

(Correct)

Item	Symbol	Condition	Rated value	Unit
Input voltage	V_I	Pxx	-0.3~7.0	V
		Pyy, #RESET	-0.3~V_{DD}+0.5	V

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S1C17 Manual errata

ITEM: Debugger Prohibition of pull-down for DSIO pin			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	3.3.3 List of debugger input/output pins	3-3
S1C17M10Technical Manual	413180200	3.3.3 List of debugger input/output pins	3-3
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	3.3.3 List of debugger input/output pins	3-3
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	3.3.3 List of debugger input/output pins	3-3
S1C17W03/W04Technical Manual	412925001	3.3.3 List of debugger input/output pins	3-3
S1C17W12/W13Technical Manual	413520201	3.3.3 List of debugger input/output pins	3-3
S1C17W14/W16Technical Manual	412910200	3.3.3 List of debugger input/output pins	3-3
S1C17W15Technical Manual	412645602	3.3.3 List of debugger input/output pins	3-3
S1C17W18Technical Manual	413129501	3.3.3 List of debugger input/output pins	3-3
S1C17W22/W23Technical Manual	412690302	3.3.3 List of debugger input/output pins	3-3
S1C17W34/W35/W36Technical Manual	413237401	3.3.3 List of debugger input/output pins	3-3
S7C17M11Technical Manual	413393900	3.3.3 List of debugger input/output pins	3-3

(Error)

3.3.3 List of Debugger Input/Output Pins

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the "I/O Ports" chapter.

Note: Do not drive the DCLK pin with a high level from outside (e.g. pulling up with a resistor). Also, do not connect (short-circuit) between the DCLK pin and another GPIO port. In the both cases, the IC may not start up normally due to unstable pin input/output status at power on.

(Correct)

3.3.3 List of Debugger Input/Output Pins

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the "I/O Ports" chapter.

Note:

- Do not drive the DCLK pin with a high level from outside (e.g. pulling up with a resistor). Also, do not connect (short-circuit) between the DCLK pin and another GPIO port. In the both cases, the IC may not start up normally due to unstable pin input/output status at power on.
- Do not drive the DSIO pin with a low level from outside. Then the CPU enters DEBUG mode by a debug interrupt.

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S1C17 Manual errata

ITEM: Real-Time Clock (RTCA) Notice of RTC Month Register			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	8.6 Control Registers	8-6
S1C17M10Technical Manual	413180200	9.6 Control Registers	9-11
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	9.6 Control Registers	9-11
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	9.6 Control Registers	9-11
S1C17W03/W04Technical Manual	412925001	9.6 Control Registers	9-11
S1C17W12/W13Technical Manual	413520201	9.6 Control Registers	9-11
S1C17W14/W16Technical Manual	412910200	9.6 Control Registers	9-11
S1C17W15Technical Manual	412645602	9.6 Control Registers	9-11
S1C17W18Technical Manual	413129501	9.6 Control Registers	9-11
S1C17W22/W23Technical Manual	412690302	9.6 Control Registers	9-11
S1C17W34/W35/W36Technical Manual	413237401	9.6 Control Registers	9-11

(Error)

RTC Month/Day Register

Bit 12 RTCMOH

Bits 11–8 RTCMOL[3:0]

The RTCMON.RTCMOH bit and the RTCMON.RTCMOL[3:0] bits are used to set and read the 10-month digit and the 1-month digit of the month counter, respectively. The setting/read values are a BCD code within the range from 1 to 12.

Note: Be sure to avoid writing to the RTCMON.RTCMOH/RTCMOL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

(Correct)

RTC Month/Day Register

Bit 12 RTCMOH

Bits 11–8 RTCMOL[3:0]

The RTCMON.RTCMOH bit and the RTCMON.RTCMOL[3:0] bits are used to set and read the 10-month digit and the 1-month digit of the month counter, respectively. The setting/read values are a BCD code within the range from 1 to 12.

Note:

- Be sure to avoid writing to the RTCMON.RTCMOH/RTCMOL[3:0] bits while the RTCCTL.RTCBSY bit = 1.
- Be sure to avoid setting 0x00 to the RTCMON.RTCMOH/RTCMOL[3:0] bits.

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S1C17 Manual errata

ITEM: Treatment of exposed die pad			
Object manuals	Document codes	Items	Pages
S1C17M01 Technical Manual	412361601	6.7.7 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-9
S1C17M10 Technical Manual	413180100	6.7.5 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-15 AP-A-9
S1C17M12/M13 Technical Manual	413454200	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-7
S1C17M30/M31/M32/M33/M34 Technical Manual	413495501	6.7.9 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-31 AP-A-23
S1C17W03/W04 Technical Manual	412924900	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-10
S1C17W13 Technical Manual	413180301	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-10
S1C17W14/W16 Technical Manual	412910200	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-11
S1C17W15 Technical Manual	412645602	6.7.5 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-14 AP-A-9
S1C17W18 Technical Manual	413129501	6.7.10 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-20 AP-A-12
S1C17W22/W23 Technical Manual	412690302	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-10

S1C17W34/W35/W36 Technical Manual	413237401	6.7.7 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-8
S7C17M11 Technical Manual	413393800	6.7.7 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-8
S1C17589 Technical Manual	412959000	6.7.12 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-22 AP-A-7

(Error)

PDIOEN (PD Port Enable Register)	15-13	-	0x00	-	R	-
	12-8	PDIEN[4:3]	0x0	H0	R/W	
	10	(reserved)	0	H0	R/W	
	9-8	PDIEN[1:0]	0x0	H0	R/W	
	7-5	-	0x00	-	R	
	4-3	PDOEN[4:3]	0x0	H0	R/W	
	2	(reserved)	0	H0	R/W	
	1-0	PDOEN[1:0]	0x0	H0	R/W	

(Correct)

PDIOEN (PD Port Enable Register)	15-13	-	0x00	-	R	-
	12-8	PDIEN[4:3]	0x0	H0	R/W	
	10	(reserved)	0	H0	R/W	
	9-8	PDIEN[1:0]	0x0	H0	R/W	
	7-5	-	0x00	-	R	
	4-0	PDOEN[4:0]	0x0	H0	R/W	

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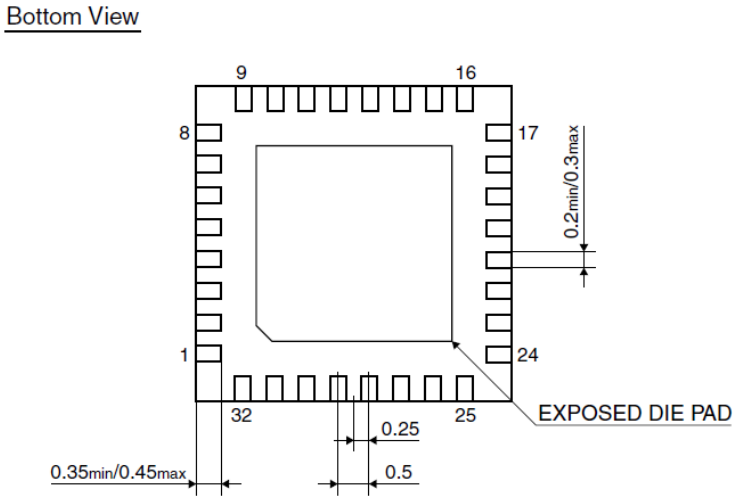
S1C17 Manual errata

ITEM: Package			
Object manuals	Document codes	Items	Pages
S1C17W03/W04 Technical Manual	412925001	23 Package	23-2
S1C17W15 Technical Manual	412645702	23 Package	23-2
S1C17W18 Technical Manual	413129601	25 Package	25-1

S1C17W03/W04 Technical Manual SQFN5-32pin

(Error)



* The potential of the EXPOSED DIE PAD is the same as that of the substrate potential (Vss) on the back of the IC.

Figure 23.2 SQFN5-32pin Package Dimensions

(Correct)

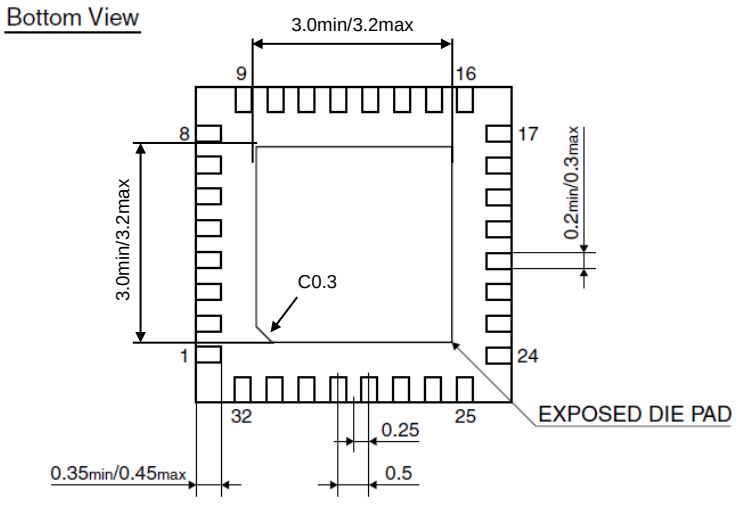


Figure 23.2 SQFN5-32pin Package Dimensions

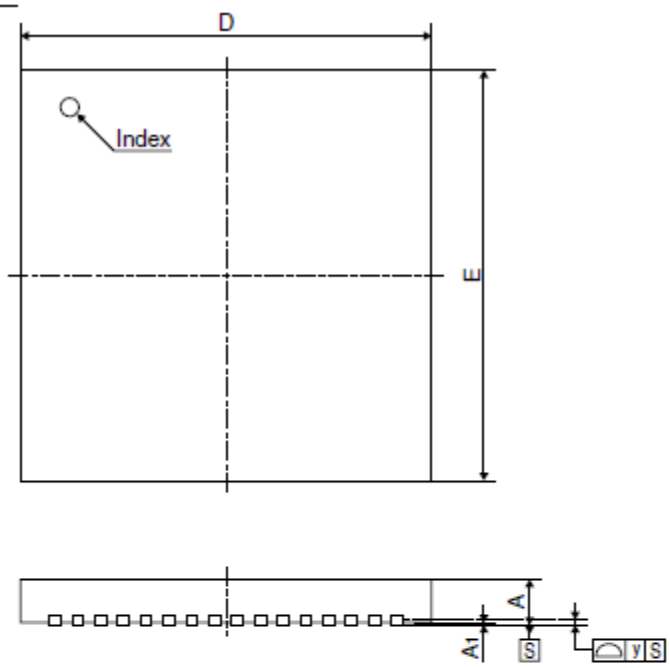
*The potential of the EXPOSED DIE PAD is the same as that of the substrate potential (VSS) on the back of the IC.

S1C17W15 Technical Manual SQFN9-64pin

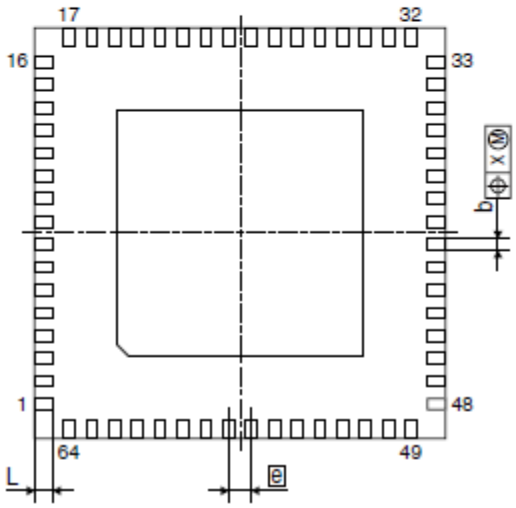
(Error)

SQFN9-64pin package

Top View



Bottom View



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	–	9	–
E	–	9	–
A	–	–	1
A_1	0	–	–
b	0.2	–	0.3
e	–	0.5	–
L	0.35	–	0.45
x	–	–	0.1
y	–	–	0.08

Figure 22.1 SQFN9-64pin Package Dimensions

(Correct)

SQFN9-64pin package

(Unit: mm)

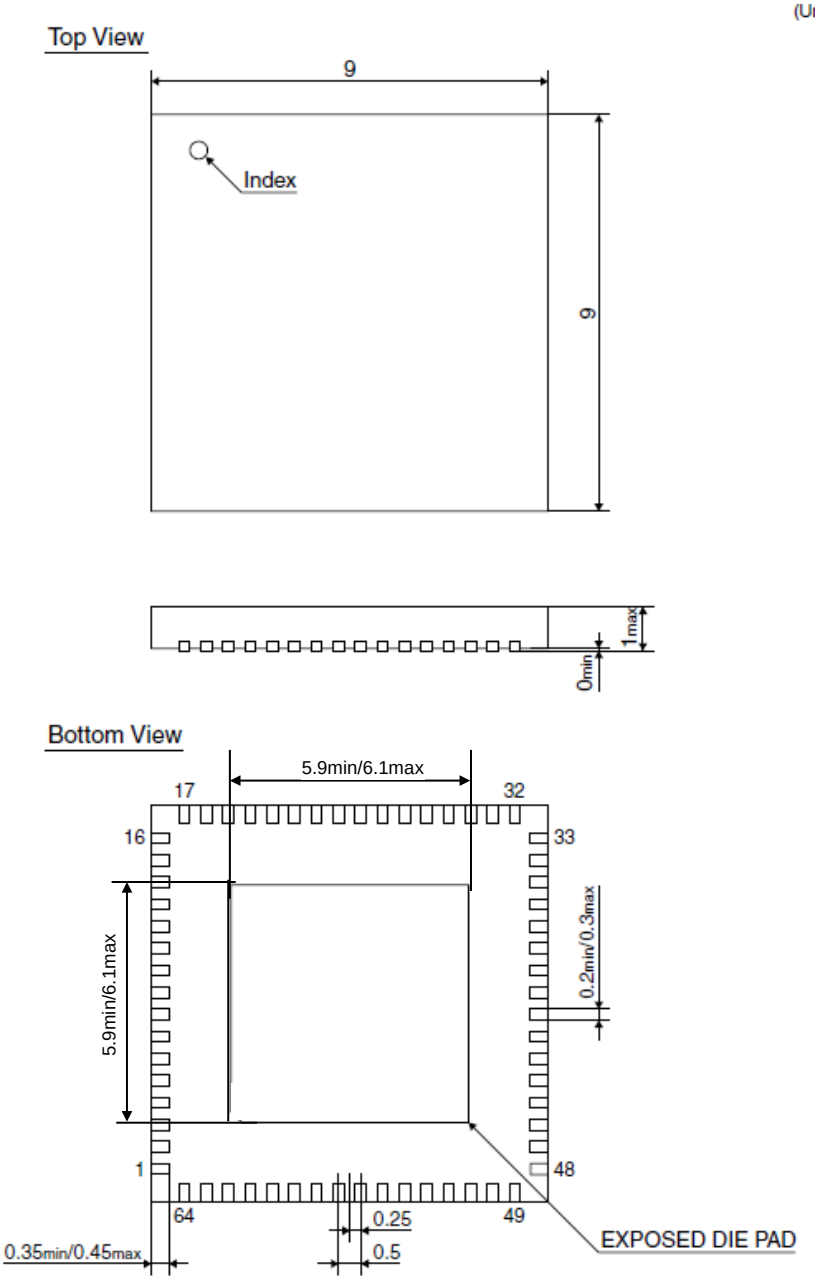
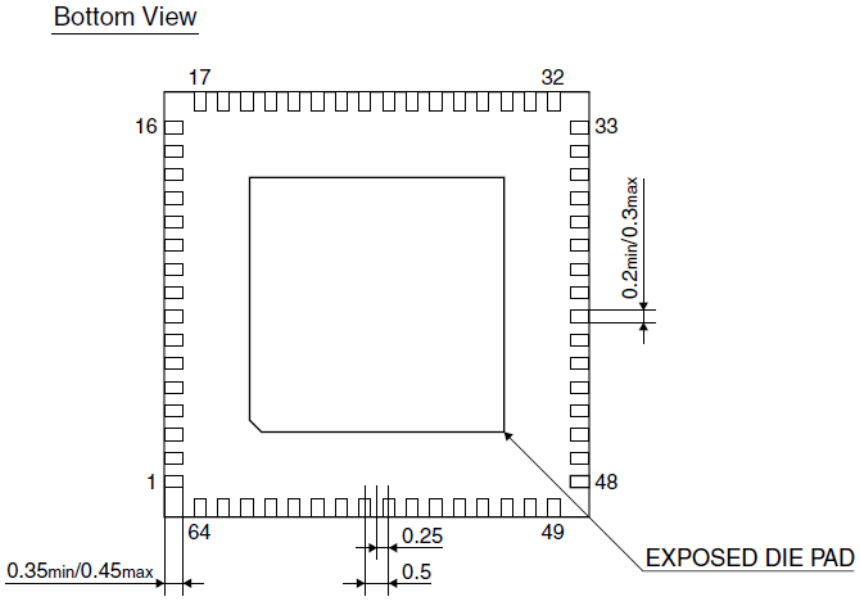


Figure 25.1 SQFN9-64pin Package Dimensions

*The potential of the EXPOSED DIE PAD is the same as that of the substrate potential (VSS) on the back of the IC.

S1C17W18 Technical Manual SQFN9-64pin package

(Error)



* The potential of the EXPOSED DIE PAD is the same as that of the substrate potential (VSS) on the back of the IC.

Figure 25.1 SQFN9-64pin Package Dimensions

(Correct)

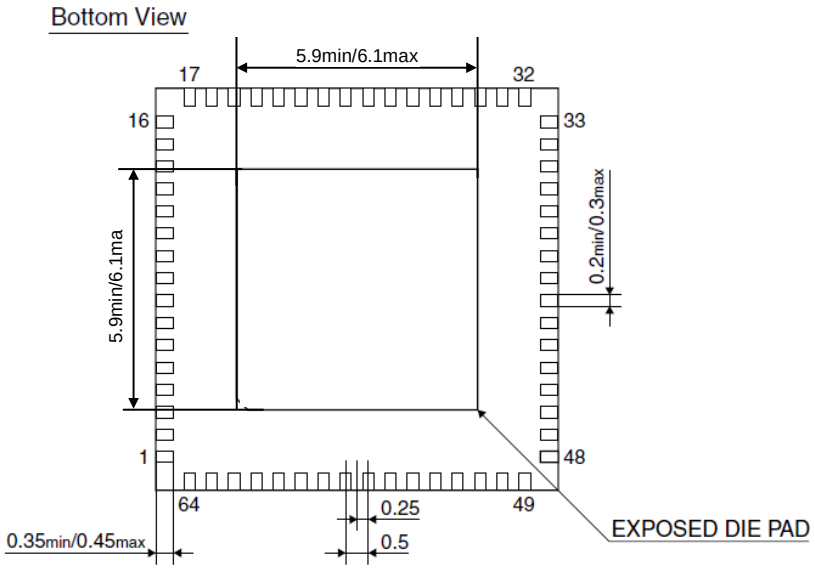


Figure 25.1 SQFN9-64pin Package Dimensions

*The potential of the EXPOSED DIE PAD is the same as that of the substrate potential (VSS) on the back of the IC.

Sep/07/2017

errata_c17w03-04_9

S1C17 Manual errata

ITEM: Treatment of exposed die pad

Object manuals	Document codes	Items	Pages
S1C17W03/W04 Technical Manual	412925001	Appendix C Mounting Precautions	AP-C-2
S1C17W15 Technical Manual	412645702	Appendix C Mounting Precautions	AP-C-2
S1C17W18 Technical Manual	413129601	Appendix C Mounting Precautions	AP-C-2
S7C17M11 Technical Manual	413393900	Appendix C Mounting Precautions	AP-C-2

(Additon)

Treatment of exposed die pad

The exposed die pad of the packages such as QFN has the same potential as that of the substrate on the back of the IC. When mounting these packages on a circuit board, please note the following:

(1) When soldering exposed die pad to mounting board

Connect the exposed die pad with a wiring pattern that has the same potential as the substrate potential on the back of the IC, or do not connect it electrically (leave it open electrically). Even if connected to the same potential on the back of the IC, the power supply pins must be connected to the power source (the exposed die pad cannot be used as a power supply pad).

(2) When not soldering exposed die pad to mounting board

Do not place any signal wiring pattern on the exposed die pad area of the mounting board.

Apr/17/2017

errata_c17w03-04_8

S1C17 Manual errata

ITEM: SVD Control

Object manuals	Document codes	Items	Pages
S1C17W03/W04 Technical Manual	412925001	10.4.1 SVD Control	10-3
S1C17W13 Technical Manual	413180401	10.4.1 SVD Control	10-3
S1C17W14/W16 Technical Manual	412910300	10.4.1 SVD Control	10-3
S1C17W15 Technical Manual	412645702	10.4.1 SVD Control	10-3
S1C17W18 Technical Manual	413129601	10.4.1 SVD Control	10-3
S1C17W22/W23 Technical Manual	412690402	10.4.1 SVD Control	10-3
S1C17W34/W35/W36 Technical Manual	413237901	10.4.1 SVD Control	10-3
S1C17M01 Technical Manual	412361701	9.4.1 SVD Control	9-3
S1C17M10 Technical Manual	413180200	10.4.1 SVD3 Control	10-3
S7C17M11 Technical Manual	413393900	9.4.1 SVD3 Control	9-3
S1C17589 Technical Manual	412959200	10.4.1 SVD Control	10-3

S1C17M10 Technical Manual, S7C17M11 Technical Manual

(Error)

4. Set the following bits when using the interrupt:
  - Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag)
  - Set the SVDINTE.SDVIE bit to 1. (Enable SVD3 interrupt)

(Correct)

4. Set the following bits when using the interrupt:
  - Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag)
  - Set the SVDINTE.SVDIE bit to 1. (Enable SVD3 interrupt)

Others

(Error) 4. Set the following bits when using the interrupt: - Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag) - Set the SVDINTE.SDVIE bit to 1. (Enable SVD interrupt)
(Correct) 4. Set the following bits when using the interrupt: - Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag) - Set the SVDINTE.SVDIE bit to 1. (Enable SVD interrupt)

Apr/17/2017

errata_c17w03-04_7

S1C17 Family Technical Manual Errata

ITEM UART (UART) Characteristics

Object manual	Document code	Object item	Page
S7C17W03/W04 Technical Manual	412925001	21.9 UART (UART) Characteristics	21-9
S1C17W13 Technical Manual	413180401	21.9 UART (UART2) Characteristics	21-10
S1C17W14/16 Technical Manual	412910300	22.9 UART (UART) Characteristics	22-9
S1C17W15 Technical Manual	412645702	20.9 UART (UART) Characteristics	20-9
S1C17W18 Technical Manual	413129601	23.9 UART (UART) Characteristics	23-9
S1C17W22/W23 Technical Manual	412690402	23.9 UART (UART) Characteristics	23-9

S1C17W13 Technical Manual

(Error)

Unless otherwise specified: V_{DD} = 1.2 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT1}	Normal mode	1.6 to 3.6 V	150	–	230,400	bps
			1.2 to 1.6 V	150	–	57,600	bps
	U_{BRT2}	IrDA mode	1.6 to 3.6 V	150	–	57,600	bps
			1.2 to 1.6 V	150	–	14,400	bps

(Correct)

Unless otherwise specified: V_{DD} = 1.2 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT1}	Normal mode	1.6 to 3.6 V	150	–	460,800	bps
			1.2 to 1.6 V	150	–	57,600	bps
	U_{BRT2}	IrDA mode	1.6 to 3.6 V	150	–	115,200	bps
			1.2 to 1.6 V	150	–	57,600	bps

Others

(Error)

Unless otherwise specified: V_{DD} = 1.2 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT1}	Normal mode	1.6 to 3.6 V	150	–	230,400	bps
			1.2 to 1.6 V	150	–	57,600	bps
	U_{BRT2}	IrDA mode	1.6 to 3.6 V	150	–	57,600	bps
			1.2 to 1.6 V	150	–	14,400	bps

(Correct)

Unless otherwise specified: V_{DD} = 1.2 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT1}	Normal mode	1.6 to 3.6 V	150	–	230,400	bps
			1.2 to 1.6 V	150	–	57,600	bps
	U_{BRT2}	IrDA mode	1.6 to 3.6 V	150	–	115,200	bps
			1.2 to 1.6 V	150	–	57,600	bps

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ITEM **16bits PWM timer (T16B)**			
Object manual	Document code	Object item	Page
S1C17589 Technical Manual	412959200	16bits PWM timer (T16B)	15-5
S1C17M10 Technical Manul	413180200		16-5
S1C17W03/W04Technical manual	412925001		15-5
S1C17W13 Technical Manual	413180401		15-5
S1C17W14/16Technical Manual	412910300		15-5
S1C17W15Technical Manual	412645702		15-5
S1C17W18Technical Manual	413129601		15-5
S1C17W22/W23 Technical Manual	412690402		15-5
S1C17W34/W35/W36 Technical Manual	413237901		15-5
S7C17M11 Technical Manual	413393900		15-5

1.1 Features

(Error)

MAX counter data register

The MAX counter data register (T16B*n*MC.MC[15:0] bits) is used to set the maximum value of the counter (hereafter referred to as MAX value). This setting limits the count range to 0x0000–MAX value and determines the count and interrupt cycles. When the counter is set to repeat mode, the MAX value can be rewritten in the procedure shown below even if the counter is running.

1. Check to see if the T16B*n*CTL.MAXBSY bit is set to 0.
2. Write the MAX value to the T16B*n*MC.MC[15:0] bits.

(Correct)

Add note statement (underlined).

MAX counter data register

The MAX counter data register (T16B*n*MC.MC[15:0] bits) is used to set the maximum value of the counter (hereafter referred to as MAX value). This setting limits the count range to 0x0000–MAX value and determines the count and interrupt cycles. When the counter is set to repeat mode, the MAX value can be rewritten in the procedure shown below even if the counter is running.

1. Check to see if the T16B*n*CTL.MAXBSY bit is set to 0.
2. Write the MAX value to the T16B*n*MC.MC[15:0] bits.

Note: When rewriting the MAX value, the new MAX value should be written after the counter has been reset to the previously set MAX value.

Dec/07/2016

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S1C17 Family Technical Manual Errata

ITEM **DCLK pin precautions**			
Object manual	Document code	Object item	Page
S1C17W03/W04 Technical Manual	412925001	3.3.3 List of debugger input/output pins	3-3
S1C17W13 Technical Manual	413180401	3.3.3 List of debugger input/output pins	3-3
S1C17W14/W16 Technical Manual	412910300	3.3.3 List of debugger input/output pins	3-3
S1C17W15 Technical Manual	412645702	3.3.3 List of debugger input/output pins	3-3
S1C17W18 Technical Manual	413129601	3.3.3 List of debugger input/output pins	3-3
S1C17W22/W23 Technical Manual	412690402	3.3.3 List of debugger input/output pins	3-3
S1C17W34/W35/W36 Technical Manual	413237901	3.3.3 List of debugger input/output pins	3-3
S1C17M01 Technical Manual	412361701	3.3.3 List of debugger input/output pins	3-3
S1C17M10 Technical Manual	413180200	3.3.3 List of debugger input/output pins	3-3
S1C17589 Technical Manual	412959200	3.3.3 List of debugger input/output pins	3-3

(Error)

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the “I/O Ports” chapter.

(Correct)

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the “I/O Ports” chapter.

Note: The DCLK pin can’t drive by high level input from external. (E.g. The pin is done pull-up etc.) Also, the DCLK pin and the other general purpose I/O pins can’t connect by a short. Because in both cases, it has possibility that the IC can’t work normally by the effect of unstable I/O at power-on.

S1C17 Family Technical Manual Errata

ITEM **I²C(I2C)**			
Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	8.6 Control Registers	8-6
S1C17F13 Technical Manual	412486301	8.6 Control Registers	8-6
S1C17W22/W23 Technical Manual	412690402	9.6 Control Registers	9-6
S1C17W15 Technical Manual	412645702	9.6 Control Registers	9-6
S1C17589 Technical Manual	412959200	9.6 Control Registers	9-6
S1C17W14/W16 Technical Manual	412910300	9.6 Control Registers	9-6
S1C17W03/W04 Technical Manual	412925001	9.6 Control Registers	9-6
S1C17W18 Technical Manual	413129601	9.6 Control Registers	9-6
S1C17M10 Technical Manual	413180200	9.6 Control Registers	9-6
S1C17W13 Technical Manual	413180401	9.6 Control Registers	9-6
S1C17W34/W35/W36 Technical Manual	413237901	9.6 Control Registers	9-6

(Error)

14.4.3 Data Reception in Master Mode

A data receiving procedure in master mode and the I2C Ch.n operations are shown below. Figures 14.4.3.1 and 14.4.3.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1. Issue a START condition by setting the I2CnCTL.TXSTART bit to 1.
2. Wait for a transmit buffer empty interrupt (I2CnINTF.TBEIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).
   Clear the I2CnINTF.STARTIF bit by writing 1 after the interrupt has occurred.
3. Write the 7-bit slave address to the I2CnTXD.TXD[7:1] bits and 1 that represents READ as the data transfer direction to the I2CnTXD.TXD0 bit.
4. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or a NACK reception interrupt (I2CnINTF.NACKIF bit=1) generated when a NACK is received.
   i. Go to Step 5 when a receive buffer full interrupt has occurred.
   ii. Clear the I2CnINTF.NACKIF bit and issue a STOP condition by setting the I2CnCTL.TXSTOP bit to 1 when a NACK reception interrupt has occurred. Then go to Step 8 or Step 1 if making a retry.
5. Perform one of the operations below when the last or next-to-last data is received.
   i. When the next-to-last data is received, write 1 to the I2CnCTL.TXNACK bit to send a NACK after the last data is received, and then go to Step 6.
   ii. When the last data is received, read the received data from the I2CnRXD register and set the

I2CnCTL.TXSTOP to 1 to generate a STOP condition. Then go to Step 8.

6. Read the received data from the I2CnRXD register.
7. Repeat Steps 4 to 6 until the end of data reception.
8. Wait for a STOP condition interrupt (I2CnINTF.STOPIF bit=1).
   Clear the I2CnINTF.STOPIF bit by writing 1 after the interrupt has occurred.

Data receiving operations

(abbrev.)

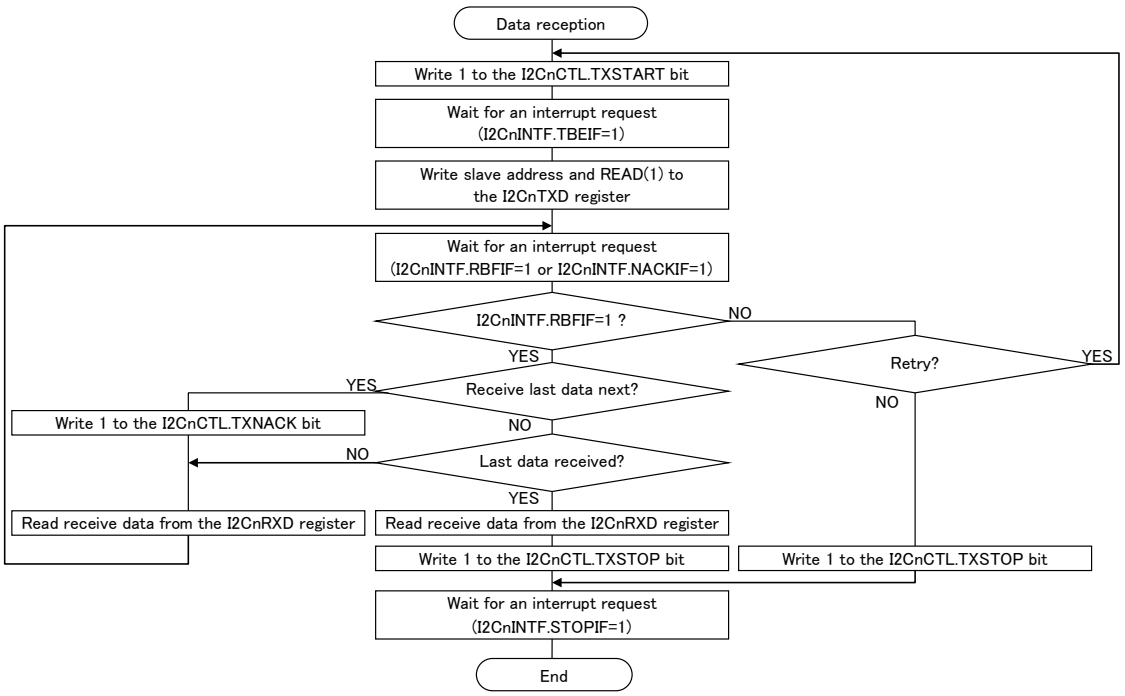

Figure 14.4.3.2 Master Mode Data Reception Flowchart

14.4.6 Data Reception in Slave Mode

A data receiving procedure in slave mode and the I2C Ch.n operations are shown below. Figures 14.4.6.1 and 14.4.6.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1. Wait for a START condition interrupt (I2CnINTF.STARTIF bit=1).
2. Check to see if the I2CnINTF.TR bit=0 (reception mode).
   (Start a data sending procedure if I2CnINTF.TR bit=1.)
3. Clear the I2CnINTF.STARTIF bit by writing 1.
4. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or an end of transfer interrupt (I2CnINTF.BYTEENDIF bit=1).
   Clear the I2CnINTF.BYTEENDIF bit by writing 1 after the interrupt has occurred.
5. If the next receive data is the last one, write 1 to the I2CnCTL.TXNACK bit to send a NACK after it is received.

6. Read the received data from the I2CnRXD register.
7. Repeat Steps 4 to 6 until the end of data reception.
8. Wait for a STOP condition interrupt (I2CnINTF.STOPIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).
   i. Go to Step 9 when a STOP condition interrupt has occurred.
   ii. Go to Step 2 when a START condition interrupt has occurred.
9. Clear the I2CnINTF.STOPIF bit and then terminate data receiving operations.

Data receiving operations

(abbrev.)

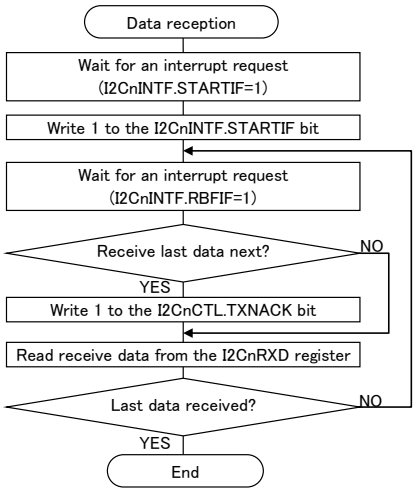

Figure 14.4.6.2 Slave Mode Data Reception Flowchart

(Correct)

14.4.3 Data Reception in Master Mode

A data receiving procedure in master mode and the I2C Ch.n operations are shown below. Figures 14.4.3.1 and 14.4.3.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1.When a one-byte reception, write 1 to the I2CnCTL.TXNACK bit.
2. Issue a START condition by setting the I2CnCTL.TXSTART bit to 1.
3. Wait for a transmit buffer empty interrupt (I2CnINTF.TBEIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).
   Clear the I2CnINTF.STARTIF bit by writing 1 after the interrupt has occurred.
4. Write the 7-bit slave address to the I2CnTXD.TXD[7:1] bits and 1 that represents READ as the data transfer direction to the I2CnTXD.TXD0 bit.
5. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or a NACK reception interrupt (I2CnINTF.NACKIF bit=1) generated when a NACK is received.

i. Go to Step 6 when a receive buffer full interrupt has occurred.

ii. Clear the I2CnINTF.NACKIF bit and issue a STOP condition by setting the I2CnCTL.TXSTOP bit to 1 when a NACK reception interrupt has occurred. Then go to Step 9 or Step 2 if making a retry.

6. Perform one of the operations below when the last or next-to-last data is received.

i. When the next-to-last data is received, write 1 to the I2CnCTL.TXNACK bit to send a NACK after the last data is received, and then go to Step 7.

ii. When the last data is received, read the received data from the I2CnRXD register and set the I2CnCTL.TXSTOP to 1 to generate a STOP condition. Then go to Step 9.

7. Read the received data from the I2CnRXD register.

8. Repeat Steps 5 to 7 until the end of data reception.

9. Wait for a STOP condition interrupt (I2CnINTF.STOPIF bit=1).
Clear the I2CnINTF.STOPIF bit by writing 1 after the interrupt has occurred.

Data receiving operations

(abbrev.)

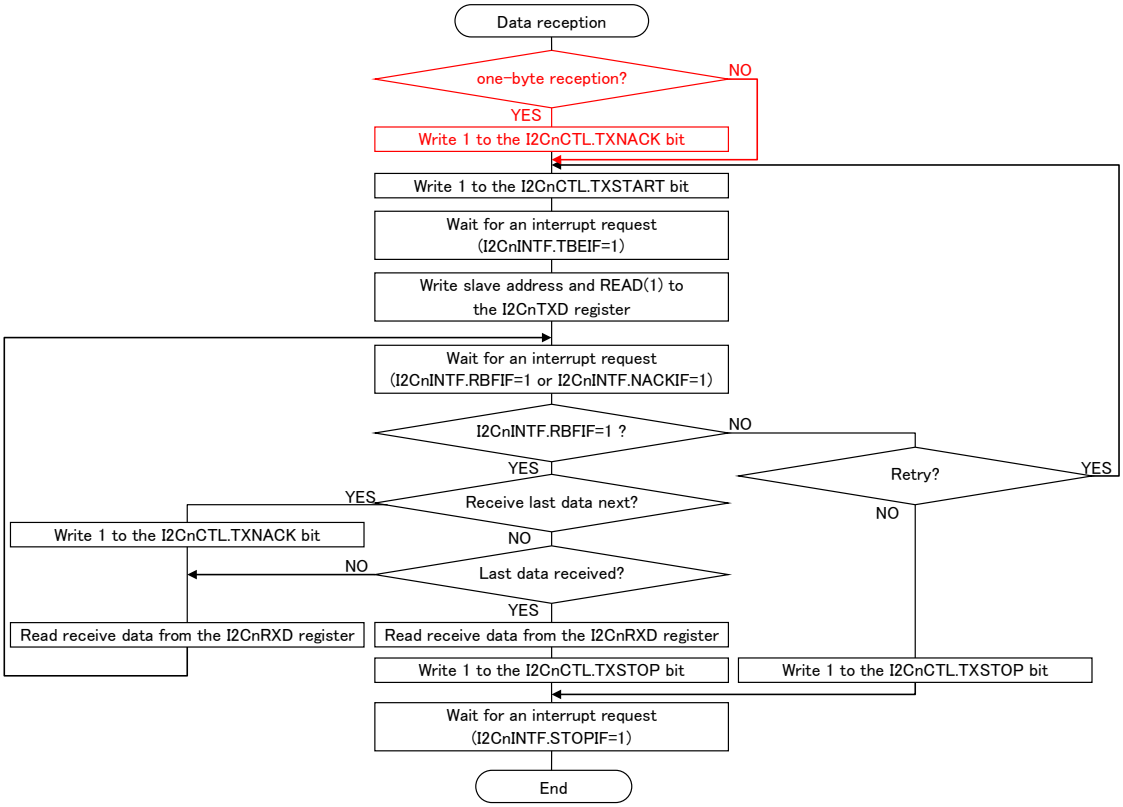

Figure 14.4.3.2 Master Mode Data Reception Flowchart

14.4.6 Data Reception in Slave Mode

A data receiving procedure in slave mode and the I2C Ch.n operations are shown below. Figures 14.4.6.1 and 14.4.6.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1.When a one-byte reception, write 1 to the I2CnCTL.TXNACK bit.

2. Wait for a START condition interrupt (I2CnINTF.STARTIF bit=1).

3. Check to see if the I2CnINTF.TR bit=0 (reception mode).
   (Start a data sending procedure if I2CnINTF.TR bit=1.)

4. Clear the I2CnINTF.STARTIF bit by writing 1.

5. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or an end of transfer interrupt (I2CnINTF.BYTEENDIF bit=1).
   Clear the I2CnINTF.BYTEENDIF bit by writing 1 after the interrupt has occurred.

6. If the next receive data is the last one, write 1 to the I2CnCTL.TXNACK bit to send a NACK after it is received.

7. Read the received data from the I2CnRXD register.

8. Repeat Steps 5 to 7 until the end of data reception.

9. Wait for a STOP condition interrupt (I2CnINTF.STOPIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).
   i. Go to Step 10 when a STOP condition interrupt has occurred.
   ii. Go to Step 3 when a START condition interrupt has occurred.

10. Clear the I2CnINTF.STOPIF bit and then terminate data receiving operations.

Data receiving operations

(abbrev.)

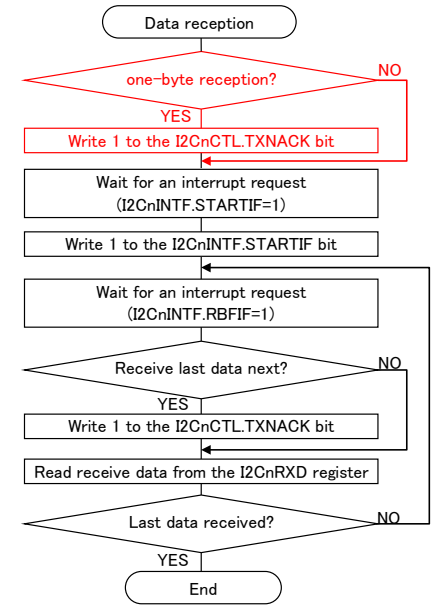

Figure 14.4.6.2 Slave Mode Data Reception Flowchart

Aug/03/2016

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S1C17 Family Technical Manual Errata

ITEM **Real-Time Clock (RTCA)**

Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	8.6 Control Registers	8-6
S1C17F13 Technical Manual	412486301	8.6 Control Registers	8-6
S1C17W22/W23 Technical Manual	412690402	9.6 Control Registers	9-6
S1C17W15 Technical Manual	412645702	9.6 Control Registers	9-6
S1C17589 Technical Manual	412959200	9.6 Control Registers	9-6
S1C17W14/W16 Technical Manual	412910300	9.6 Control Registers	9-6
S1C17W03/W04 Technical Manual	412925001	9.6 Control Registers	9-6
S1C17W18 Technical Manual	413129601	9.6 Control Registers	9-6
S1C17M10 Technical Manual	413180200	9.6 Control Registers	9-6
S1C17W13 Technical Manual	413180401	9.6 Control Registers	9-6
S1C17W34/W35/W36 Technical Manual	413237901	9.6 Control Registers	9-6

(Error)

Bits14–8 RTCTRM[6:0]

Write the correction value for adjusting the 1 Hz frequency to these bits to execute theoretical regulation.For a calculation method of correction value, refer to “Theoretical Regulation Function.”

Note: When the RTCCTL.RTCTRMBSY bit = 1, the RTCCTL.RTCTRM[6:0] bits cannot be rewritten.

(Correct)

Bits14–8 RTCTRM[6:0]

Write the correction value for adjusting the 1 Hz frequency to these bits to execute theoretical regulation.For a calculation method of correction value, refer to “Theoretical Regulation Function.”

Notes: ・When the RTCCTL.RTCTRMBSY bit = 1, the RTCCTL.RTCTRM[6:0] bits cannot be rewritten.

・When 0x00 is written to the RTCCTL.RTCTRM[6:0] bits, the RTCCTL.RTCTRMBSY bit goes 1, but the time-of-day clock is not corrected.

Aug/03/2016

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S1C17 Family Technical Manual Errata

ITEM **Watchdog Timer (WDT)**

Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	7.4 Control Registers	7-3~4
S1C17F13 Technical Manual	412486301	7.4 Control Registers	7-3~4
S1C17W22/W23 Technical Manual	412690402	8.4 Control Registers	8-3~4
S1C17W15 Technical Manual	412645702	8.4 Control Registers	8-3~4
S1C17589 Technical Manual	412959200	8.4 Control Registers	8-3~4
S1C17W14/W16 Technical Manual	412910300	8.4 Control Registers	8-3~4
S1C17W03/W04 Technical Manual	412925001	8.4 Control Registers	8-3~4
S1C17W18 Technical Manual	413129601	8.4 Control Registers	8-3~4

(Error)

Bits 3–0 WDTRUN[3:0]

These bits control WDT to run and stop.

0xa (R/WP): Stop

Values other than 0xa (R/WP): Run

Always 0x0 is read if a value other than 0xa is written.

Since a reset may be generated immediately after running depending on the counter value, WDT should also be reset concurrently when running WDT.

(Correct)

Bits 3–0 WDTRUN[3:0]

These bits control WDT to run and stop.

0xa (WP): Stop

Values other than 0xa (WP): Run

0xa (R): Stopping

0x0 (R): Running

Always 0x0 is read if a value other than 0xa is written.

Since a reset may be generated immediately after running depending on the counter value, WDT should also be reset concurrently when running WDT.

S1C17 Family Technical Manual Errata

ITEM **External connection for VPP**			
Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	**4.3.3 Flash Programming** **17.2 Recommended Operating Conditions** **18 Basic External Connection Diagram**	4-3 17-1 18-1
S1C17W03/04 Technical Manual	412925001	**4.3.3 Flash Programming** **21.2 Recommended Operating Conditions** **22 Basic External Connection Diagram**	4-3 21-1 22-1
S1C17W14/16 Technical Manual	412910300	**4.3.3 Flash Programming** **22.2 Recommended Operating Conditions** **23 Basic External Connection Diagram**	4-3 22-1 23-1
S1C17W15 Technical Manual	412645702	**4.3.3 Flash Programming** **20.2 Recommended Operating Conditions** **21 Basic External Connection Diagram**	4-3 20-1 21-1
S1C17W22/23 Technical Manual	412690402	**4.3.3 Flash Programming** **23.2 Recommended Operating Conditions** **24 Basic External Connection Diagram**	4-3 23-1 24-1
S1C17589 Technical Manual	412959200	**4.3.3 Flash Programming** **19.2 Recommended Operating Conditions** **20 Basic External Connection Diagram**	4-3 19-1 20-1
S1C17656 Technical Manual	412745100	**3.2.2 Flash Programming**	3-2

Flash Programming

(Error)

(S1C17M01)

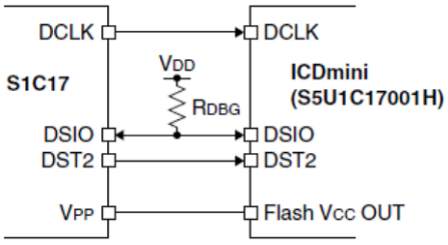


Figure 4.3.3.1 External Connection

(Exclude S1C17M01,S1C17656)

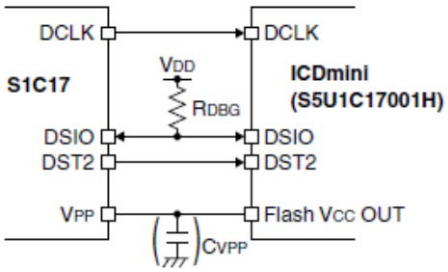


Figure 4.3.3.1 External Connection

The VPP pin must be left open except when programming the Flash memory. However, it is not necessary to disconnect the wire when using ICDmini to supply the VPP power, as ICDmini controls the power supply so that it will be supplied during Flash programming only. CVPP should be connected if the VPP voltage is not

stable due to the effect of the distance between the VPP and Flash VCC OUT or other causes.

(Correct)

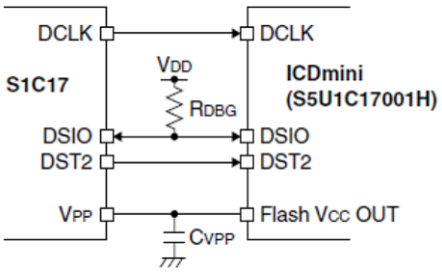


Figure 4.3.3.1 External Connection

The VPP pin must be left open except when programming the Flash memory. However, it is not necessary to disconnect the wire when using ICDmini to supply the VPP voltage, as ICDmini controls the power supply so that it will be supplied during Flash programming only. Be sure to connect CVPP for stabilizing the voltage when the VPP voltage is supplied externally.

Flash Programming (Only S1C17656)

(Error)

The S1C17656 supports on-board programming of the Flash memory, it makes it possible to program the Flash memory with the application programs/data by using the debugger through an ICDmini.

(Correct)

The S1C17656 supports on-board programming of the Flash memory, it makes it possible to program the Flash memory with the application programs/data by using the debugger through an ICDmini. Be sure to connect CVPP for stabilizing the voltage when the VPP voltage is supplied externally.

Recommended Operating Conditions

(Error)

(S1C17M01)

No description

(Exclude S1C17M01)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Capacitor between VSS and VPP	CVPP	* ※	–	0.1	–	μF

*※ CVPP should be connected only when the VPP voltage is not stable.

(※ is 4-6)

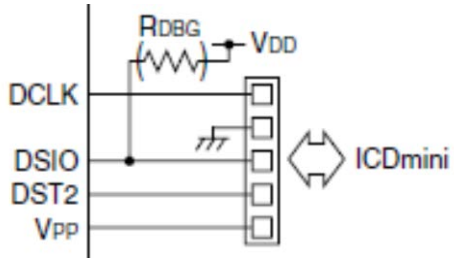
(Correct)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Capacitor between VSS and VPP	CVPP		–	0.1	–	μF

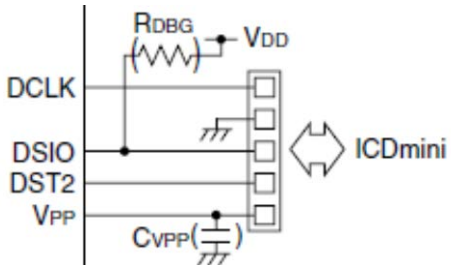
Basic External Connection Diagram

(Error)

(S1C17M01)



(Exclude S1C17M01)



(Correct)