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errata_c17w18_26

S1C17 Manual errata

ITEM: Corrective operation when a value out of the effective range is set			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	8.4.2 Real-Time Clock Counter Operations	8-4
S1C17M10Technical Manual	413180200	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17M20/M21/M22/M23/M24/M25Technical Manual	413557000	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17M30/M31/M32/M33/M34Technical Manual	413495601	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17M40Technical Manual	413895200	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W03/W04Technical Manual	412925001	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W12/13Technical Manual	413520201	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W14/W16Technical Manual	412910300	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W15Technical Manual	412645702	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W18Technical Manual	413129601	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W22/W23Technical Manual	412690402	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17W34/W35/W36Technical Manual	413237901	9.4.2 Real-Time Clock Counter Operations	9-4
S1C17F63Technical Manual	413942900	21.4.2Real-Time Clock Function	21-6

(Error)

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing.

(Correct)

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing of the counter. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing of the counter.

Note: RTCMON.RTCMOH bits=0 & RTCMON.RTCMOL[3:0] bits=0x0 are prohibited.

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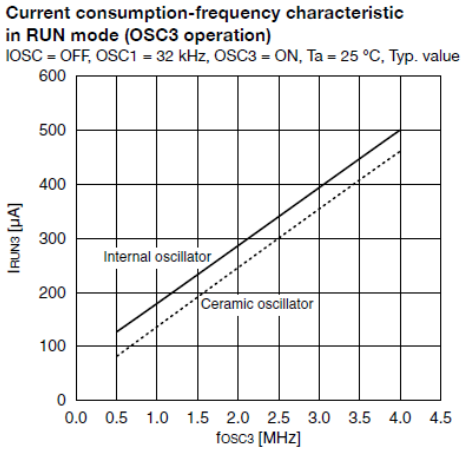
S1C17 Manual errata

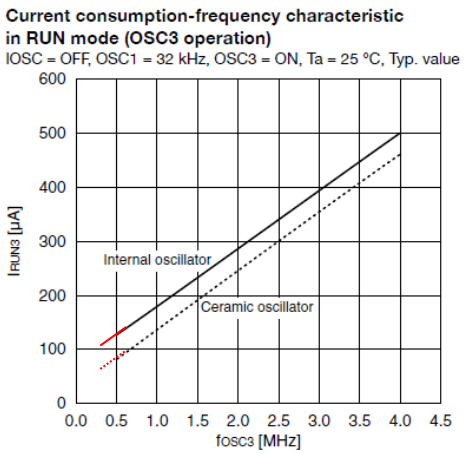
ITEM: Current consumption-frequency characteristics in RUN mode (OSC3 operation)			
Object manuals	Document codes	Items	Pages
S1C17W18 Technical Manual	413129601	23.3 Current Consumption	23-3
S1C17W34/W35/W36 Technical Manual	413237901	23.3 Current Consumption	23-3
S1C17W12/W13 Technical Manual	413520201	21.3 Current Consumption	21-3

S1C17W12/W13/W18

(Error)



(Correct)

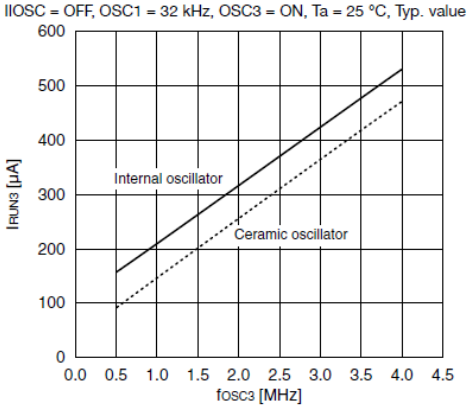


S1C17W34/W35/W36

(Error)

Current consumption-frequency characteristic in RUN mode (OSC3 operation)

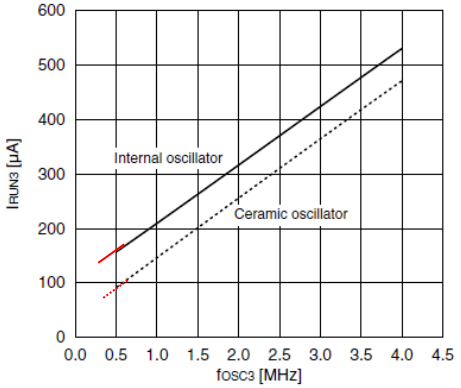
IIOSC = OFF, OSC1 = 32 kHz, OSC3 = ON, Ta = 25 °C, Typ. value



(Correct)

Current consumption-frequency characteristic in RUN mode (OSC3 operation)

IIOSC = OFF, OSC1 = 32 kHz, OSC3 = ON, Ta = 25 °C, Typ. value



Nov/25/2019

errata_c17w18_24

S1C17 Manual errata

ITEM: Real-Time Clock (RTCA) Theoretical Regulation Function			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	8.3.2 Theoretical Regulation Function	8-2
S1C17M10Technical Manual	413180200	9.3.2 Theoretical Regulation Function	9-2
S1C17M20/M21/M22/M23/M24 /M25 Technical Manual	413557000	9.3.2 Theoretical Regulation Function	9-2
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	9.3.2 Theoretical Regulation Function	9-2
S1C17W03/W04Technical Manual	412925001	9.3.2 Theoretical Regulation Function	9-2
S1C17W12/W13Technical Manual	413520201	9.3.2 Theoretical Regulation Function	9-2
S1C17W14/W16Technical Manual	412910200	9.3.2 Theoretical Regulation Function	9-2
S1C17W15Technical Manual	412645602	9.3.2 Theoretical Regulation Function	9-2
S1C17W18Technical Manual	413129501	9.3.2 Theoretical Regulation Function	9-2
S1C17W22/W23Technical Manual	412690302	9.3.2 Theoretical Regulation Function	9-2
S1C17W34/W35/W36Technical Manual	413237401	9.3.2 Theoretical Regulation Function	9-2

(Error)

9.3.2 Theoretical Regulation Function

The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.

1. Measure the frequency tolerance "m [ppm]" of f_{OSC1}.
2. Determine the theoretical regulation execution cycle time "n seconds."
3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2.
4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt.
5. Monitor the RTC1S signal to check that every n-second cycle has no error included.

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two's-complement number. Use Eq. 9.1 to calculate the correction value.

n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.
RTCTRM[6:0] bits periodically via software)
m: OSC1 frequency tolerance [ppm]

(Correct)

9.3.2 Theoretical Regulation Function

The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.

1. Determine the correction value of frequency tolerance "m [ppm] =- {(fOSC1-32768[Hz]) / 32768[Hz]}×10⁶" by measuring the f_{OSC1}.
2. Determine the theoretical regulation execution cycle time "n seconds."
3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2.
4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt.
5. Monitor the RTC1S signal to check that every n-second cycle has no error included.

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two's-complement number. Use Eq. 9.1 to calculate the correction value.

n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.
RTCTRM[6:0] bits periodically via software)
m: OSC1's correction value of frequency tolerance [ppm]

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ITEM: Reset hold circuit characteristics			
Object manuals	Document codes	Items	Pages
S1C17M10Technical Manual	413180200	19.4 System Reset Controller (SRC) Characteristics	19-3
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	21.4 System Reset Controller (SRC) Characteristics	21-4
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	23.4 System Reset Controller (SRC) Characteristics	23-4
S1C17W03/W04Technical Manual	412925001	21.4 System Reset Controller (SRC) Characteristics	21-4
S1C17W12/W13Technical Manual	413520201	21.4 System Reset Controller (SRC) Characteristics	21-4
S1C17W14/W16Technical Manual	412910200	22.4 System Reset Controller (SRC) Characteristics	22-4
S1C17W15Technical Manual	412645602	20.4 System Reset Controller (SRC) Characteristics	20-4
S1C17W18Technical Manual	413129501	23.4 System Reset Controller (SRC) Characteristics	23-4
S1C17W22/W23Technical Manual	412690302	23.4 System Reset Controller (SRC) Characteristics	23-4
S1C17W34/W35/W36Technical Manual	413237401	23.4 System Reset Controller (SRC) Characteristics	23-4
S7C17M11Technical Manual	413393900	21.4 System Reset Controller (SRC) Characteristics	21-4

S1C17M10/M20/M21/M22/M23/M24/M25/M30/M31/M32/M33/M34/S7C17M11

(Error)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		-	-	200	uS

(Correct)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		0.5	-	0.9	mS

S1C17W03/W04/W12/W13/W15/W14/W16/W18/W22/W23/W34/W35/W36

(Error)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		-	-	1.7	mS

(Correct)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	tRSTR		0.5	-	0.9	mS

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ITEM: Absolute Maximum Ratings of #RESET pin

Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	17.1 Absolute Maximum Ratings	17-1
S1C17M10Technical Manual	413180200	19.1 Absolute Maximum Ratings	19-1
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	21.1 Absolute Maximum Ratings	21-1
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	23.1 Absolute Maximum Ratings	23-1
S1C17W03/W04Technical Manual	412925001	21.1 Absolute Maximum Ratings	21-1
S1C17W12/W13Technical Manual	413520201	21.1 Absolute Maximum Ratings	21-1
S1C17W14/W16Technical Manual	412910200	22.1 Absolute Maximum Ratings	22-1
S1C17W15Technical Manual	412645602	20.1 Absolute Maximum Ratings	20-1
S1C17W18Technical Manual	413129501	23.1Absolute Maximum Ratings	23-1
S1C17W22/W23Technical Manual	412690302	23.1Absolute Maximum Ratings	23-1
S1C17W34/W35/W36Technical Manual	413237401	23.1Absolute Maximum Ratings	23-1
S7C17M11Technical Manual	413393900	21.1Absolute Maximum Ratings	21-1

(Error)

Item	Symbol	Condition	Rated value	Unit
Input voltage	V_I	Pxx	-0.3~7.0	V
		Pyy	-0.3~V_{DD}+0.5	V

(Correct)

Item	Symbol	Condition	Rated value	Unit
Input voltage	V_I	Pxx	-0.3~7.0	V
		Pyy, #RESET	-0.3~V_{DD}+0.5	V

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ITEM: Debugger Prohibition of pull-down for DSIO pin			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	3.3.3 List of debugger input/output pins	3-3
S1C17M10Technical Manual	413180200	3.3.3 List of debugger input/output pins	3-3
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	3.3.3 List of debugger input/output pins	3-3
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	3.3.3 List of debugger input/output pins	3-3
S1C17W03/W04Technical Manual	412925001	3.3.3 List of debugger input/output pins	3-3
S1C17W12/W13Technical Manual	413520201	3.3.3 List of debugger input/output pins	3-3
S1C17W14/W16Technical Manual	412910200	3.3.3 List of debugger input/output pins	3-3
S1C17W15Technical Manual	412645602	3.3.3 List of debugger input/output pins	3-3
S1C17W18Technical Manual	413129501	3.3.3 List of debugger input/output pins	3-3
S1C17W22/W23Technical Manual	412690302	3.3.3 List of debugger input/output pins	3-3
S1C17W34/W35/W36Technical Manual	413237401	3.3.3 List of debugger input/output pins	3-3
S7C17M11Technical Manual	413393900	3.3.3 List of debugger input/output pins	3-3

(Error)

3.3.3 List of Debugger Input/Output Pins

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the "I/O Ports" chapter.

Note: Do not drive the DCLK pin with a high level from outside (e.g. pulling up with a resistor). Also, do not connect (short-circuit) between the DCLK pin and another GPIO port. In the both cases, the IC may not start up normally due to unstable pin input/output status at power on.

(Correct)

3.3.3 List of Debugger Input/Output Pins

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the "I/O Ports" chapter.

Note:

- Do not drive the DCLK pin with a high level from outside (e.g. pulling up with a resistor). Also, do not connect (short-circuit) between the DCLK pin and another GPIO port. In the both cases, the IC may not start up normally due to unstable pin input/output status at power on.
- Do not drive the DSIO pin with a low level from outside. Then the CPU enters DEBUG mode by a debug interrupt.

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ITEM: Real-Time Clock (RTCA) Notice of RTC Month Register			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361701	8.6 Control Registers	8-6
S1C17M10Technical Manual	413180200	9.6 Control Registers	9-11
S1C17M20/M21/M22/M23/M24/M25 Technical Manual	413557000	9.6 Control Registers	9-11
S1C17M30/M31/M32/M33/M34 Technical Manual	413495600	9.6 Control Registers	9-11
S1C17W03/W04Technical Manual	412925001	9.6 Control Registers	9-11
S1C17W12/W13Technical Manual	413520201	9.6 Control Registers	9-11
S1C17W14/W16Technical Manual	412910200	9.6 Control Registers	9-11
S1C17W15Technical Manual	412645602	9.6 Control Registers	9-11
S1C17W18Technical Manual	413129501	9.6 Control Registers	9-11
S1C17W22/W23Technical Manual	412690302	9.6 Control Registers	9-11
S1C17W34/W35/W36Technical Manual	413237401	9.6 Control Registers	9-11

(Error)

RTC Month/Day Register

Bit 12 RTCMOH

Bits 11–8 RTCMOL[3:0]

The RTCMON.RTCMOH bit and the RTCMON.RTCMOL[3:0] bits are used to set and read the 10-month digit and the 1-month digit of the month counter, respectively. The setting/read values are a BCD code within the range from 1 to 12.

Note: Be sure to avoid writing to the RTCMON.RTCMOH/RTCMOL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

(Correct)

RTC Month/Day Register

Bit 12 RTCMOH

Bits 11–8 RTCMOL[3:0]

The RTCMON.RTCMOH bit and the RTCMON.RTCMOL[3:0] bits are used to set and read the 10-month digit and the 1-month digit of the month counter, respectively. The setting/read values are a BCD code within the range from 1 to 12.

Note:

- Be sure to avoid writing to the RTCMON.RTCMOH/RTCMOL[3:0] bits while the RTCCTL.RTCBSY bit = 1.
- Be sure to avoid setting 0x00 to the RTCMON.RTCMOH/RTCMOL[3:0] bits.

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ITEM: Recommended Operating Conditions LCD power supply voltage

Object manuals	Document codes	Items	Pages
S1C17M10Technical Manual	413180200	19.2 Recommended Operating Conditions	19-1
S1C17W12/W13Technical Manual	413520201	21.2 Recommended Operating Conditions	21-1
S1C17W14/W16Technical Manual	412910200	21.2 Recommended Operating Conditions	22-1
S1C17W15Technical Manual	412645602	21.2 Recommended Operating Conditions	20-1
S1C17W18Technical Manual	413129501	21.2 Recommended Operating Conditions	23-1
S1C17W22/W23Technical Manual	412690302	21.2 Recommended Operating Conditions	23-1
S1C17W34/W35/W36Technical Manual	413237401	21.2 Recommended Operating Conditions	23-1

S1C17W12/W13/W14/W16

(Error)

項目	記号	条件	Min.	Typ.	Max.	単位
LCD power supply voltage	V_{C1}	When an external voltage is applied, $V_{C1} \leqq V_{C2} \leqq V_{C3}$	-	1.0	1.8	V
	V_{C2}		-	2.0	3.6	V
	V_{C3}		-	3.0	5.4	V

(Correct)

項目	記号	条件	Min.	Typ.	Max.	単位
LCD power supply voltage	V_{C1}	When an external voltage is applied, $V_{C1} \leqq V_{C2} \leqq V_{C3}$, $V_{C1} \leqq V_{DD}$	-	1.0	1.8	V
	V_{C2}		-	2.0	3.6	V
	V_{C3}		-	3.0	5.4	V

S1C17W15/W18/W22/W23

(Error)

項目	記号	条件	Min.	Typ.	Max.	単位
LCD power supply voltage（1/3bias）	V_{C1}	When an external voltage is applied, $V_{C1} \leqq V_{DD} \leqq V_{C2} \leqq V_{C3} (= V_{C4})$	-	1.0	1.8	V
	V_{C2}		-	2.0	3.6	V
	V_{C3}/V_{C4}		-	3.0	5.4	V
LCD power supply voltage（1/4bias）	V_{C1}	When an external voltage is applied, $V_{C1} \leqq V_{DD} \leqq V_{C2} \leqq V_{C3} \leqq V_{C4}$	-	1.0	1.4	V
	V_{C2}		-	2.0	2.8	V
	V_{C3}		-	3.0	4.2	V
	V_{C4}		-	4.0	5.6	V

(Correct)

項目	記号	条件	Min.	Typ.	Max.	単位
LCD power supply voltage（1/3bias）	V_{C1}	When an external voltage is applied, $V_{C1} \leqq V_{C2} \leqq V_{C3} (= V_{C4})$, $V_{C1} \leqq V_{DD}$	-	1.0	1.8	V
	V_{C2}		-	2.0	3.6	V
	V_{C3}/V_{C4}		-	3.0	5.4	V
LCD power supply voltage（1/4bias）	V_{C1}	When an external voltage is applied, $V_{C1} \leqq V_{C2} \leqq V_{C3} \leqq V_{C4}$, $V_{C1} \leqq V_{DD}$	-	1.0	1.4	V
	V_{C2}		-	2.0	2.8	V
	V_{C3}		-	3.0	4.2	V
	V_{C4}		-	4.0	5.6	V

S1C17M10/W34/W35/W36

(Error)

項目	記号	条件	Min.	Typ.	Max.	単位
LCD power supply voltage（1/4bias）	V_{C1}	When an external voltage is applied, $V_{C1} \leqq V_{DD} \leqq V_{C2} \leqq V_{C3} \leqq V_{C4} (= V_{C5})$	-	1.0	1.2	V
	V_{C2}		-	2.0	2.4	V
	V_{C3}		-	3.0	3.6	V
	V_{C4}/V_{C5}		-	4.0	4.8	V
LCD power supply voltage（1/5bias）	V_{C1}	When an external voltage is applied, $V_{C1} \leqq V_{DD} \leqq V_{C2} \leqq V_{C3} \leqq V_{C4} \leqq V_{C5}$	-	1.0	1.2	V
	V_{C2}		-	2.0	2.4	V
	V_{C3}			3.0	3.6	V
	V_{C4}		-	4.0	4.8	V
	V_{C5}		-	5.0	6.0	V

(Correct)

項目	記号	条件	Min.	Typ.	Max.	単位
LCD power supply voltage（1/4bias）	V_{C1}	When an external voltage is applied, $V_{C1} \leqq V_{C2} \leqq V_{C3} \leqq V_{C4} (= V_{C5})$, $V_{C2} \leqq V_{DD}$	-	1.0	1.2	V
	V_{C2}		-	2.0	2.4	V
	V_{C3}		-	3.0	3.6	V
	V_{C4}/V_{C5}		-	4.0	4.8	V
LCD power supply voltage（1/5bias）	V_{C1}	When an external voltage is applied, $V_{C1} \leqq V_{C2} \leqq V_{C3} \leqq V_{C4} \leqq V_{C5}$, $V_{C2} \leqq V_{DD}$	-	1.0	1.2	V
	V_{C2}		-	2.0	2.4	V
	V_{C3}			3.0	3.6	V
	V_{C4}		-	4.0	4.8	V
	V_{C5}		-	5.0	6.0	V

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ITEM: LCD Driver List of Output Pins

Object manuals	Document codes	Items	Pages
S1C17M10Technical Manual	413180100	17.2.1 List of Output Pins	17-2
S1C17M30/M31/M32/M33/M34Technical Manual	413495501	18.2.1 List of Output Pins	18-3
S1C17W13Technical Manual	413180301	18.2.1 List of Output Pins	18-2
S1C17W14/W16Technical Manual	412910200	16.2.1 List of Output Pins	18-2
S1C17W15Technical Manual	412645602	17.2.1 List of Output Pins	17-2
S1C17W18Technical Manual	413129501	18.2.1 List of Output Pins	18-2
S1C17W22/W23Technical Manual	412690302	18.2.1 List of Output Pins	18-2
S1C17W34/W35/W36Technical Manual	413237401	18.2.1 List of Output Pins	18-2
S7C17M11Technical Manual	413393800	17.2.1 List of Output Pins	17-2

S1C17M10Technical Manual

(Error)

The COM8-15 outputs and SEG87-80 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note: Be sure to avoid using the VC1 to VC5 pin outputs for driving external circuits.

(Correct)

The COM8-15 outputs and SEG87-80 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note:

- **Be sure to avoid using the VC1 to VC5 pin outputs for driving external circuits.**
- **When LCD panel is connected, LCD16CTL.LCDDIS bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.**

S1C17M30/M31/M32/M33/M34 Technical Manual, S7C17M11 Technical Manual

(Error)

The COM4–7 outputs and SEG0–4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note: Be sure to avoid using the VC1 to VC3 pin outputs of the model with an embedded LCD power supply for driving external circuits.

(Correct)

The COM4–7 outputs and SEG0–4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note:

- **Be sure to avoid using the VC1 to VC3 pin outputs of the model with an embedded LCD power supply for driving external circuits.**
- **When LCD panel is connected, LCD8CTL.LCDDIS bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.**

S1C17W13 Technical Manual

(Error)

If the port is shared with the LCD4A pin and other functions, the LCD4A output function must be assigned to the port before activating the LCD4A. For more information, refer to the "I/O Ports" chapter.

Note: Be sure to avoid using the VC1 to VC3 pin outputs for driving external circuits.

(Correct)

If the port is shared with the LCD4A pin and other functions, the LCD4A output function must be assigned to the port before activating the LCD4A. For more information, refer to the "I/O Ports" chapter.

Note:

- **Be sure to avoid using the VC1 to VC3 pin outputs for driving external circuits.**
- **When LCD panel is connected, LCD4CTL.LCDDIS bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.**

S1C17W14/W16Technical Manual, S1C17W18Technical Manual

(Error)

The COM4–7 outputs and SEG0–4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note: Be sure to avoid using the VC1 to VC3 pin outputs for driving external circuits

(Correct)

The COM4–7 outputs and SEG0–4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note:

- **Be sure to avoid using the VC1 to VC3 pin outputs for driving external circuits**
- **When LCD panel is connected, LCD8CTL.LCDDIS bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.**

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(Error)

The COM4–7 outputs and SEG0–4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note: Be sure to avoid using the VC1 to VC4 pin outputs for driving external circuits.

(Correct)

The COM4–7 outputs and SEG0–4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note:

- **Be sure to avoid using the VC1 to VC4 pin outputs for driving external circuits.**
- **When LCD panel is connected, LCD8CTL.MODEN bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.**

S1C17W22/W23Technical Manual

(Error)

If the port is shared with the LCD24A pin and other functions, the LCD24A output function must be assigned to the port before activating the LCD24A. For more information, refer to the "I/O Ports" chapter.

Note: Be sure to avoid using the VC1 to VC4 pin outputs for driving external circuits.

(Correct)

f the port is shared with the LCD24A pin and other functions, the LCD24A output function must be assigned to the port before activating the LCD24A. For more information, refer to the "I/O Ports" chapter.

Note:

- **Be sure to avoid using the VC1 to VC4 pin outputs for driving external circuits.**
- **When LCD panel is connected, LCD24CTL.MODEN bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.**

S1C17W34/W35/W36Technical Manual

(Error)

The COM16-31 outputs and SEG0-15 or SEG79-64 outputs share the pins. Selecting a drive duty and COM[31:16] pin location switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note: Be sure to avoid using the VC1 to VC5 pin outputs for driving external circuits.

(Correct)

The COM16-31 outputs and SEG0-15 or SEG79-64 outputs share the pins. Selecting a drive duty and COM[31:16] pin location switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note:

- **Be sure to avoid using the VC1 to VC5 pin outputs for driving external circuits.**
- **When LCD panel is connected, LCD32CTL.MODEN bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.**

Sep/07/2017

errata_c17w18_16

S1C17 Manual errata

ITEM: LCD Driver List of Output Pins			
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361601	14.2.1 List of Output Pins	14-2
S1C17M10Technical Manual	413180100	17.2.1 List of Output Pins	17-2
S1C17M30/M31/M32/M33/M34Technical Manual	413495501	18.2.1 List of Output Pins	18-3
S1C17W13Technical Manual	413180301	18.2.1 List of Output Pins	18-2
S1C17W14/W16Technical Manual	412910200	16.2.1 List of Output Pins	18-2
S1C17W15Technical Manual	412645602	17.2.1 List of Output Pins	17-2
S1C17W18Technical Manual	413129501	18.2.1 List of Output Pins	18-2
S1C17W22/W23Technical Manual	412690302	18.2.1 List of Output Pins	18-2
S1C17W34/W35/W36Technical Manual	413237401	18.2.1 List of Output Pins	18-2
S7C17M11Technical Manual	413393800	17.2.1 List of Output Pins	17-2

S1C17M01 Technical Manual

(Error)

Table 14.2.1.1 List of LCD8A Pins

Pin name	I/O*	Initial status*	Function
SEG31–0	O	O (L)	Segment data output pin
COM7–0	O	O (L)	Common data output pin
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin

* Indicates the status when the pin is configured for LCD8A.

(Correct)

Table 14.2.1.1 List of LCD8A Pins

Pin name	I/O*	Initial status*	Function
SEG31–0	A	O (L)	Segment data output pin
COM7–0	A	O (L)	Common data output pin
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin

* Indicates the status when the pin is configured for LCD8A.

S1C17M10 Technical Manual

(Error)

Table 17.2.1.1 List of LCD16A Pins

Pin name	I/O*1	Initial status*1	Function
COM0–7	O	Hi-Z / O (L)*2	Common data output pins
COM8–15/SEG87–80	O	Hi-Z / O (L)*2	General purpose IO/common data output/segment data output pins
SEG0–68	O	Hi-Z / O (L)*2	Segment data output pins
SEG69–79	O	Hi-Z / O (L)*2	General purpose IO/segment data output pins
LFRO	O	O (L)	Frame signal monitoring output pin
$V_{C1–5}$	P	–	LCD panel drive power supply pins
$C_{P1–5}$	A	–	LCD voltage booster capacitor connecting pins

*1: Indicates the status when the pin is configured for LCD16A. *2: When LCD16CTL.LCDDIS bit = 1

(Correct)

Table 17.2.1.1 List of LCD16A Pins

Pin name	I/O*1	Initial status*1	Function
COM0–7	A	Hi-Z / O (L)*2	Common data output pins
COM8–15/SEG87–80	A	Hi-Z / O (L)*2	General purpose IO/common data output/segment data output pins
SEG0–68	A	Hi-Z / O (L)*2	Segment data output pins
SEG69–79	A	Hi-Z / O (L)*2	General purpose IO/segment data output pins
LFRO	O	O (L)	Frame signal monitoring output pin
$V_{C1–5}$	P	–	LCD panel drive power supply pins
$C_{P1–5}$	A	–	LCD voltage booster capacitor connecting pins

*1: Indicates the status when the pin is configured for LCD16A. *2: When LCD16CTL.LCDDIS bit = 1

S1C17M30/M31/M32/M33/M34 Technical Manual

(Error)

Table 18.2.1.1 List of LCD8A Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	A	Hi-Z / O (V_{SS})*2	Common data output pins
COM4–7/SEG0–3	A	Hi-Z / O (V_{SS})*2	Common data output/segment data output pins
SEG4–49	A	Hi-Z / O (V_{SS})*2	Segment data output pins (See Table 18.2.1.2.)
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin (S1C17M31/M33/M34)
C_{P2}	A	–	LCD voltage booster capacitor connecting pin (S1C17M31/M33/M34)

*1: Indicates the status when the pin is configured for LCD8A. *2: When LCD8CTL.LCDDIS bit = 1

(Correct)

Table 18.2.1.1 List of LCD8A Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	A	Hi-Z / O (V_{SS})*2	Common data output pins
COM4–7/SEG0–3	A	Hi-Z / O (V_{SS})*2	Common data output/segment data output pins
SEG4–49	A	Hi-Z / O (V_{SS})*2	Segment data output pins (See Table 18.2.1.2.)
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin (S1C17M31/M33/M34)
C_{P2}	A	–	LCD voltage booster capacitor connecting pin (S1C17M31/M33/M34)

*1: Indicates the status when the pin is configured for LCD8A. *2: When LCD8CTL.LCDDIS bit = 1

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(Error)

Table 18.2.1.1 List of LCD4A Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	O	Hi-Z / O (L)*2	Common data output-only pins
SEG0–1	O	Hi-Z / O (L)*2	Segment data output-only pins (Not available in the SQFN7-48pin package)
SEG2–7	O	Hi-Z / O (L)*2	Segment data output-only pins
SEG8–19	O	Hi-Z / O (L)*2	General-purpose IO/segment data output pins
SEG20–21	O	Hi-Z / O (L)*2	Segment data output-only pins (Not available in the 48-pin package)
SEG22–25	O	Hi-Z / O (L)*2	General-purpose IO/segment data output pins (Not available in the 48-pin package)
LFRO	O	O (L)	Frame signal monitoring output pin (Not available in the TQFP12-48pin package)
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin (Not available in the TQFP12-48pin package)
C_{P2}	A	–	LCD voltage booster capacitor connecting pin (Not available in the TQFP12-48pin package)

*1: Indicates the status when the pin is configured for LCD4A. *2: When LCD4CTL.LCDDIS bit = 1

(Correct)

Table 18.2.1.1 List of LCD4A Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	A	Hi-Z / O (L)*2	Common data output-only pins
SEG0–1	A	Hi-Z / O (L)*2	Segment data output-only pins (Not available in the SQFN7-48pin package)
SEG2–7	A	Hi-Z / O (L)*2	Segment data output-only pins
SEG8–19	A	Hi-Z / O (L)*2	General-purpose IO/segment data output pins
SEG20–21	A	Hi-Z / O (L)*2	Segment data output-only pins (Not available in the 48-pin package)
SEG22–25	A	Hi-Z / O (L)*2	General-purpose IO/segment data output pins (Not available in the 48-pin package)
LFRO	O	O (L)	Frame signal monitoring output pin (Not available in the TQFP12-48pin package)
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin (Not available in the TQFP12-48pin package)
C_{P2}	A	–	LCD voltage booster capacitor connecting pin (Not available in the TQFP12-48pin package)

*1: Indicates the status when the pin is configured for LCD4A. *2: When LCD4CTL.LCDDIS bit = 1

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(Error)

Table 18.2.1.1 List of LCD8B Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	O	Hi-Z / O (L)*2	Common data output-only pin
COM4–7/SEG0–3	O	Hi-Z / O (L)*2	Common data output/segment data output pin
SEG4–41(W14) SEG4–46(W16)	O	Hi-Z / O (L)*2	Segment data output-only pin
SEG42–53(W14) SEG47–59(W16)	O	Hi-Z / O (L)*2	General-purpose IO/segment data output pin
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin

*1: Indicates the status when the pin is configured for LCD8B. *2: When LCD8CTL.LCDDIS bit = 1

(Correct)

Table 18.2.1.1 List of LCD8B Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	A	Hi-Z / O (L)*2	Common data output-only pin
COM4–7/SEG0–3	A	Hi-Z / O (L)*2	Common data output/segment data output pin
SEG4–41(W14) SEG4–46(W16)	A	Hi-Z / O (L)*2	Segment data output-only pin
SEG42–53(W14) SEG47–59(W16)	A	Hi-Z / O (L)*2	General-purpose IO/segment data output pin
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin

*1: Indicates the status when the pin is configured for LCD8B. *2: When LCD8CTL.LCDDIS bit = 1

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(Error)

Table 17.2.1.1 List of LCD8B Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	O	Hi-Z / O (L)*2	Common data output-only pin
COM4–7/SEG0–3	O	Hi-Z / O (L)*2	Common data output/segment data output pin
SEG4–15	O	Hi-Z / O (L)*2	Segment data output-only pin
SEG16–23	O	O (L)	General-purpose IO/segment data output pin
SEG24–27	O	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin package)
SEG28–29	O	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin/80-pin package)
SEG30–33	O	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin package)
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
V_{C4}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin
C_{P3}	A	–	LCD voltage booster capacitor connecting pin
C_{P4}	A	–	LCD voltage booster capacitor connecting pin

*1: Indicates the status when the pin is configured for LCD8B. *2: When LCD8CTL.MODEN bit = 1

(Correct)

Table 17.2.1.1 List of LCD8B Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	A)	Hi-Z / O (L)*2	Common data output-only pin
COM4–7/SEG0–3	A)	Hi-Z / O (L)*2	Common data output/segment data output pin
SEG4–15	A)	Hi-Z / O (L)*2	Segment data output-only pin
SEG16–23	A)	O (L)	General-purpose IO/segment data output pin
SEG24–27	A)	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin package)
SEG28–29	A)	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin/80-pin package)
SEG30–33	A)	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin package)
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
V_{C4}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin
C_{P3}	A	–	LCD voltage booster capacitor connecting pin
C_{P4}	A	–	LCD voltage booster capacitor connecting pin

*1: Indicates the status when the pin is configured for LCD8B. *2: When LCD8CTL.MODEN bit = 1

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(Error)

Table 18.2.1.1 List of LCD8B Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	O	Hi-Z / O (L)*2	General-purpose IO/Common data output-only pin
COM4–7/SEG0–3	O	Hi-Z / O (L)*2	General-purpose IO/Common data output/segment data output pin
SEG4–23	O	Hi-Z / O (L)*2	General-purpose IO/segment data output pin
SEG24–27	O	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin package)
SEG28–34	O	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin/80-pin package)
SEG35–38	O	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin package)
SEG39–47	O	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin/80-pin package)
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
V_{C4}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin
C_{P3}	A	–	LCD voltage booster capacitor connecting pin
C_{P4}	A	–	LCD voltage booster capacitor connecting pin

*1: Indicates the status when the pin is configured for LCD8B. *2: When LCD8CTL.LCDDIS bit = 1

(Correct)

Table 18.2.1.1 List of LCD8B Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	A	Hi-Z / O (L)*2	General-purpose IO/Common data output-only pin
COM4–7/SEG0–3	A	Hi-Z / O (L)*2	General-purpose IO/Common data output/segment data output pin
SEG4–23	A	Hi-Z / O (L)*2	General-purpose IO/segment data output pin
SEG24–27	A	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin package)
SEG28–34	A	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin/80-pin package)
SEG35–38	A	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin package)
SEG39–47	A	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin/80-pin package)
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
V_{C4}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin
C_{P3}	A	–	LCD voltage booster capacitor connecting pin
C_{P4}	A	–	LCD voltage booster capacitor connecting pin

*1: Indicates the status when the pin is configured for LCD8B. *2: When LCD8CTL.LCDDIS bit = 1

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(Error)

Table 18.2.1.1 List of LCD24A Pins

Pin name	I/O*1	Initial status*1	Function
SEG53–0	O	Hi-Z / O (L)*2	Segment data output-only pin
COM7–0	O	Hi-Z / O (L)*2	Common data output-only pin
SEG71–54	O	O (L)	General-purpose IO/segment data output pin
COM23–8	O	O (L)	General-purpose IO/common data output pin
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
V_{C4}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin
C_{P3}	A	–	LCD voltage booster capacitor connecting pin
C_{P4}	A	–	LCD voltage booster capacitor connecting pin

*1: Indicates the status when the pin is configured for LCD24A. *2: When LCD24CTL.MODEN bit = 1

(Correct)

Table 18.2.1.1 List of LCD24A Pins

Pin name	I/O*1	Initial status*1	Function
SEG53–0	A	Hi-Z / O (L)*2	Segment data output-only pin
COM7–0	A	Hi-Z / O (L)*2	Common data output-only pin
SEG71–54	A	O (L)	General-purpose IO/segment data output pin
COM23–8	A	O (L)	General-purpose IO/common data output pin
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
V_{C4}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin
C_{P3}	A	–	LCD voltage booster capacitor connecting pin
C_{P4}	A	–	LCD voltage booster capacitor connecting pin

*1: Indicates the status when the pin is configured for LCD24A. *2: When LCD24CTL.MODEN bit = 1

S1C17W34/W35/W36 Technical Manual

(Error)

Table 18.2.1.1 List of LCD32B Pins

Pin name	I/O*1	Initial status*1	Function
COM0–15	O	Hi-Z / O (L)*2	Common data output-only pins
SEG0–15/COM16–31	O	Hi-Z / O (L)*2	Segment data output/common data output pins
SEG16–63	O	Hi-Z / O (L)*2	Segment data output-only pin
SEG64–79/COM31–16	O	Hi-Z / O (L)*2	Segment data output/common data output pins
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}–V_{C5}	P	–	LCD panel drive power supply pins
C_{P1}–C_{P5}	A	–	LCD voltage booster capacitor connecting pins

*1: Indicates the status when the pin is configured for LCD32B. *2: When LCD32CTL.LCDDIS bit = 1

(Correct)

Table 18.2.1.1 List of LCD32B Pins

Pin name	I/O*1	Initial status*1	Function
COM0–15	A	Hi-Z / O (L)*2	Common data output-only pins
SEG0–15/COM16–31	A	Hi-Z / O (L)*2	Segment data output/common data output pins
SEG16–63	A	Hi-Z / O (L)*2	Segment data output-only pin
SEG64–79/COM31–16	A	Hi-Z / O (L)*2	Segment data output/common data output pins
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}–V_{C5}	P	–	LCD panel drive power supply pins
C_{P1}–C_{P5}	A	–	LCD voltage booster capacitor connecting pins

*1: Indicates the status when the pin is configured for LCD32B. *2: When LCD32CTL.LCDDIS bit = 1

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(Error)

Table 17.2.1.1 List of LCD8A Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	O	Hi-Z / O (L)*2	Common data output pin
COM4–7/SEG0–3	O	Hi-Z / O (L)*2	Common data output/segment data output pin
SEG4–33	O	Hi-Z / O (L)*2	Segment data output pin
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin

*1: Indicates the status when the pin is configured for LCD8A. *2: When LCD8CTL.LCDDIS bit = 1

(Correct)

Table 17.2.1.1 List of LCD8A Pins

Pin name	I/O*1	Initial status*1	Function
COM0–3	A)	Hi-Z / O (L)*2	Common data output pin
COM4–7/SEG0–3	A)	Hi-Z / O (L)*2	Common data output/segment data output pin
SEG4–33	A)	Hi-Z / O (L)*2	Segment data output pin
LFRO	O	O (L)	Frame signal monitoring output pin
V_{C1}	P	–	LCD panel drive power supply pin
V_{C2}	P	–	LCD panel drive power supply pin
V_{C3}	P	–	LCD panel drive power supply pin
C_{P1}	A	–	LCD voltage booster capacitor connecting pin
C_{P2}	A	–	LCD voltage booster capacitor connecting pin

*1: Indicates the status when the pin is configured for LCD8A. *2: When LCD8CTL.LCDDIS bit = 1

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S1C17 Manual errata

ITEM: Treatment of exposed die pad			
Object manuals	Document codes	Items	Pages
S1C17M01 Technical Manual	412361601	6.7.7 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-9
S1C17M10 Technical Manual	413180100	6.7.5 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-15 AP-A-9
S1C17M12/M13 Technical Manual	413454200	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-7
S1C17M30/M31/M32/M33/M34 Technical Manual	413495501	6.7.9 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-31 AP-A-23
S1C17W03/W04 Technical Manual	412924900	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-10
S1C17W13 Technical Manual	413180301	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-10
S1C17W14/W16 Technical Manual	412910200	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-11
S1C17W15 Technical Manual	412645602	6.7.5 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-14 AP-A-9
S1C17W18 Technical Manual	413129501	6.7.10 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-20 AP-A-12
S1C17W22/W23 Technical Manual	412690302	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-10

S1C17W34/W35/W36 Technical Manual	413237401	6.7.7 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-8
S7C17M11 Technical Manual	413393800	6.7.7 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-8
S1C17589 Technical Manual	412959000	6.7.12 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-22 AP-A-7

(Error)

PDIOEN (PD Port Enable Register)	15-13	-	0x00	-	R	-
	12-8	PDIEN[4:3]	0x0	H0	R/W	
	10	(reserved)	0	H0	R/W	
	9-8	PDIEN[1:0]	0x0	H0	R/W	
	7-5	-	0x00	-	R	
	4-3	PDOEN[4:3]	0x0	H0	R/W	
	2	(reserved)	0	H0	R/W	
	1-0	PDOEN[1:0]	0x0	H0	R/W	

(Correct)

PDIOEN (PD Port Enable Register)	15-13	-	0x00	-	R	-
	12-8	PDIEN[4:3]	0x0	H0	R/W	
	10	(reserved)	0	H0	R/W	
	9-8	PDIEN[1:0]	0x0	H0	R/W	
	7-5	-	0x00	-	R	
	4-0	PDOEN[4:0]	0x0	H0	R/W	

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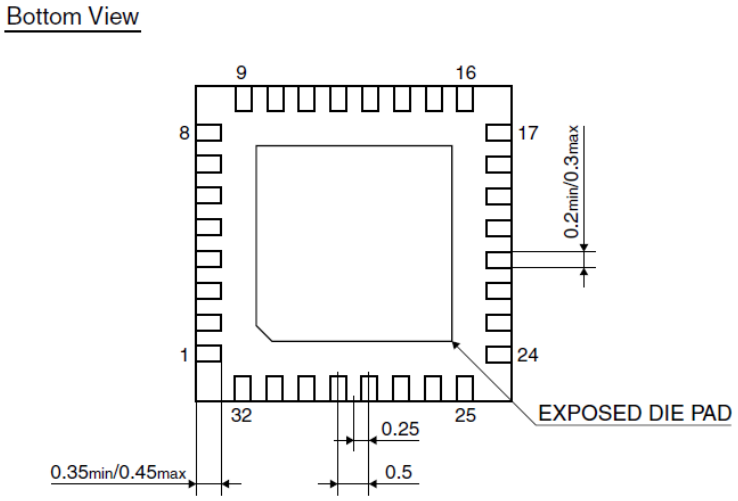
errata_c17w18_14

S1C17 Manual errata

ITEM: Package			
Object manuals	Document codes	Items	Pages
S1C17W03/W04 Technical Manual	412925001	23 Package	23-2
S1C17W15 Technical Manual	412645702	23 Package	23-2
S1C17W18 Technical Manual	413129601	25 Package	25-1

S1C17W03/W04 Technical Manual SQFN5-32pin

(Error)



* The potential of the EXPOSED DIE PAD is the same as that of the substrate potential (Vss) on the back of the IC.

Figure 23.2 SQFN5-32pin Package Dimensions

(Correct)

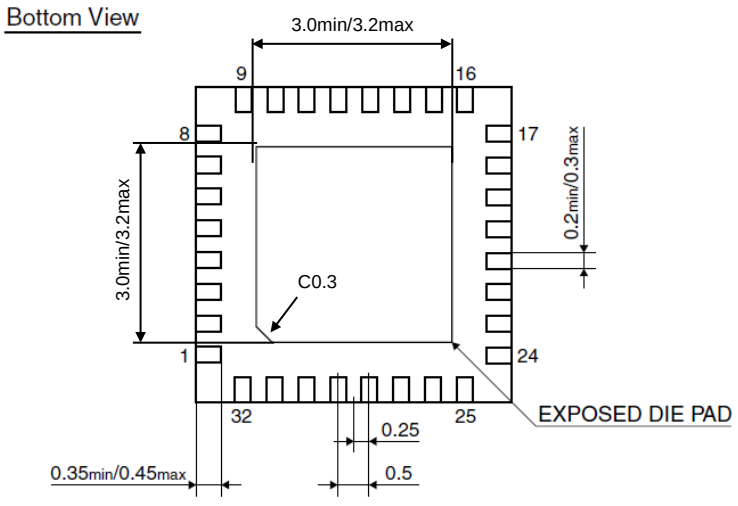


Figure 23.2 SQFN5-32pin Package Dimensions

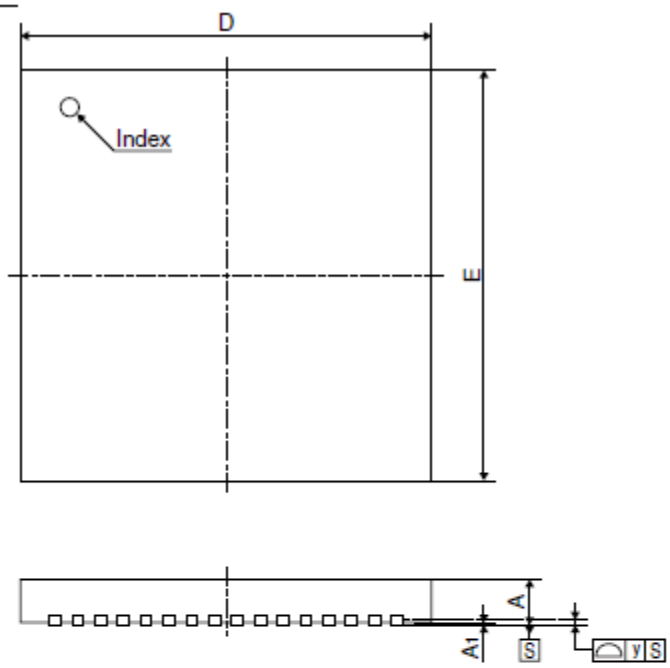
*The potential of the EXPOSED DIE PAD is the same as that of the substrate potential (VSS) on the back of the IC.

S1C17W15 Technical Manual SQFN9-64pin

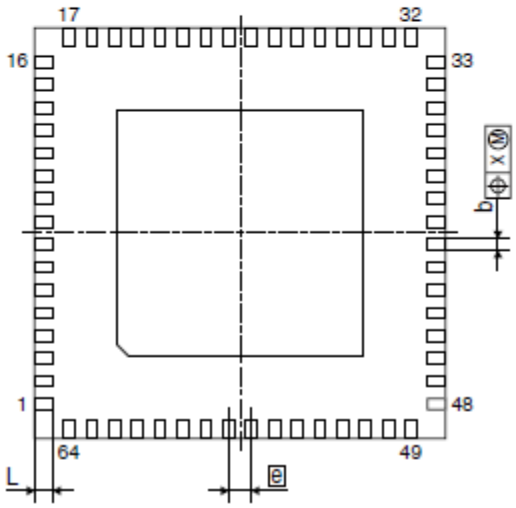
(Error)

SQFN9-64pin package

Top View



Bottom View



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	–	9	–
E	–	9	–
A	–	–	1
A_1	0	–	–
b	0.2	–	0.3
e	–	0.5	–
L	0.35	–	0.45
x	–	–	0.1
y	–	–	0.08

Figure 22.1 SQFN9-64pin Package Dimensions

(Correct)

SQFN9-64pin package

(Unit: mm)

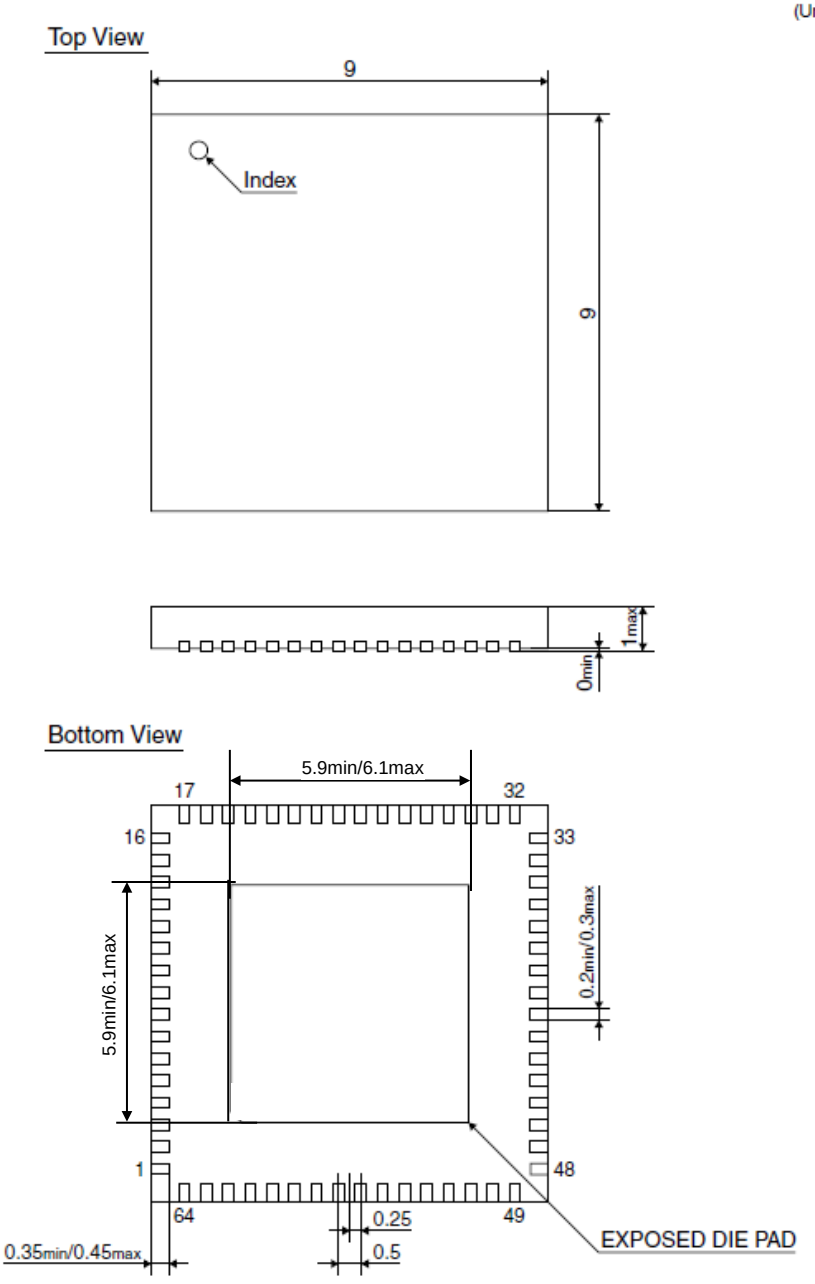
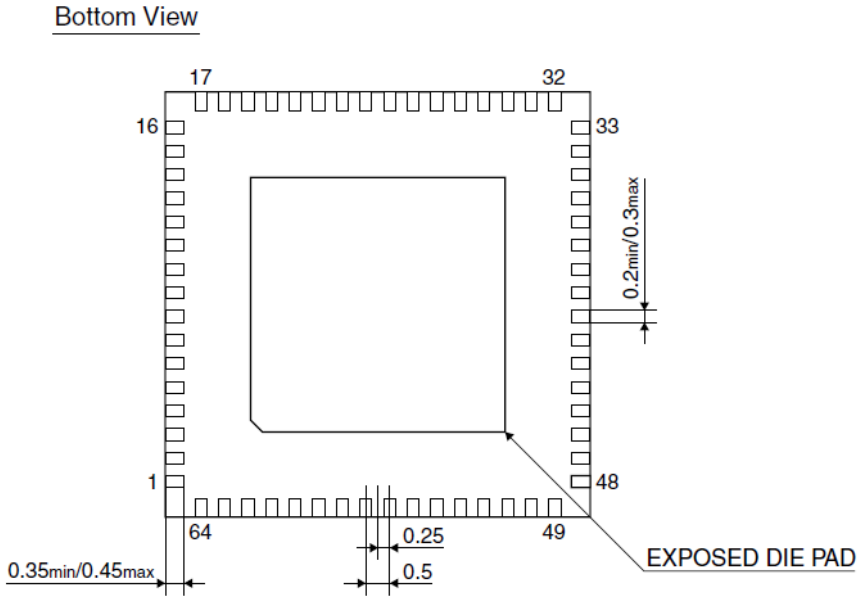


Figure 25.1 SQFN9-64pin Package Dimensions

*The potential of the EXPOSED DIE PAD is the same as that of the substrate potential (VSS) on the back of the IC.

S1C17W18 Technical Manual SQFN9-64pin package

(Error)



* The potential of the EXPOSED DIE PAD is the same as that of the substrate potential (VSS) on the back of the IC.

Figure 25.1 SQFN9-64pin Package Dimensions

(Correct)

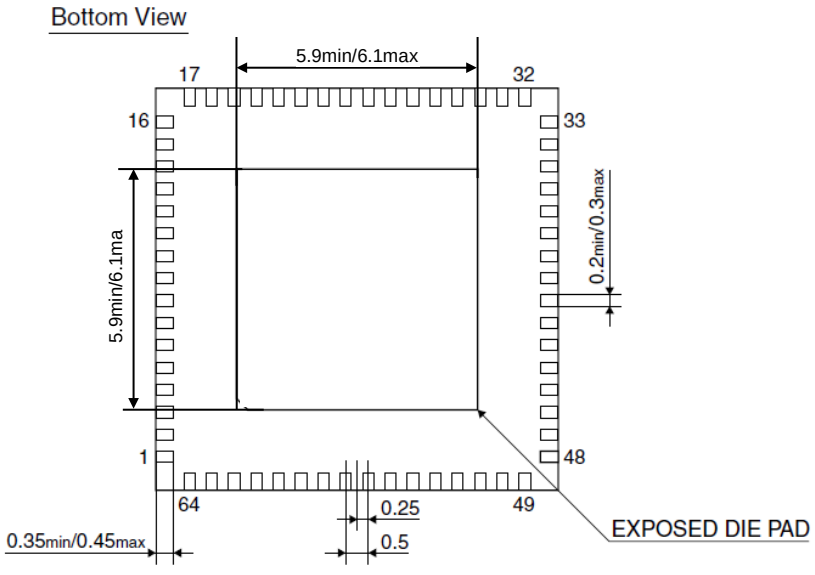


Figure 25.1 SQFN9-64pin Package Dimensions

*The potential of the EXPOSED DIE PAD is the same as that of the substrate potential (VSS) on the back of the IC.

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S1C17 Manual errata

ITEM: Treatment of exposed die pad

Object manuals	Document codes	Items	Pages
S1C17W03/W04 Technical Manual	412925001	Appendix C Mounting Precautions	AP-C-2
S1C17W15 Technical Manual	412645702	Appendix C Mounting Precautions	AP-C-2
S1C17W18 Technical Manual	413129601	Appendix C Mounting Precautions	AP-C-2
S7C17M11 Technical Manual	413393900	Appendix C Mounting Precautions	AP-C-2

(Additon)

Treatment of exposed die pad

The exposed die pad of the packages such as QFN has the same potential as that of the substrate on the back of the IC. When mounting these packages on a circuit board, please note the following:

(1) When soldering exposed die pad to mounting board

Connect the exposed die pad with a wiring pattern that has the same potential as the substrate potential on the back of the IC, or do not connect it electrically (leave it open electrically). Even if connected to the same potential on the back of the IC, the power supply pins must be connected to the power source (the exposed die pad cannot be used as a power supply pad).

(2) When not soldering exposed die pad to mounting board

Do not place any signal wiring pattern on the exposed die pad area of the mounting board.

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S1C17 Manual errata

ITEM: SVD Control

Object manuals	Document codes	Items	Pages
S1C17W03/W04 Technical Manual	412925001	10.4.1 SVD Control	10-3
S1C17W13 Technical Manual	413180401	10.4.1 SVD Control	10-3
S1C17W14/W16 Technical Manual	412910300	10.4.1 SVD Control	10-3
S1C17W15 Technical Manual	412645702	10.4.1 SVD Control	10-3
S1C17W18 Technical Manual	413129601	10.4.1 SVD Control	10-3
S1C17W22/W23 Technical Manual	412690402	10.4.1 SVD Control	10-3
S1C17W34/W35/W36 Technical Manual	413237901	10.4.1 SVD Control	10-3
S1C17M01 Technical Manual	412361701	9.4.1 SVD Control	9-3
S1C17M10 Technical Manual	413180200	10.4.1 SVD3 Control	10-3
S7C17M11 Technical Manual	413393900	9.4.1 SVD3 Control	9-3
S1C17589 Technical Manual	412959200	10.4.1 SVD Control	10-3

S1C17M10 Technical Manual, S7C17M11 Technical Manual

(Error)

4. Set the following bits when using the interrupt:
  - Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag)
  - Set the SVDINTE.SDVIE bit to 1. (Enable SVD3 interrupt)

(Correct)

4. Set the following bits when using the interrupt:
  - Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag)
  - Set the SVDINTE.SVDIE bit to 1. (Enable SVD3 interrupt)

Others

(Error) 4. Set the following bits when using the interrupt: - Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag) - Set the SVDINTE.SDVIE bit to 1. (Enable SVD interrupt)
(Correct) 4. Set the following bits when using the interrupt: - Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag) - Set the SVDINTE.SVDIE bit to 1. (Enable SVD interrupt)

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errata_c17w18_11

S1C17 Family Technical Manual Errata

errata_c17w18_6 are revised.

ITEM

Object manual	Document code	Object item	Page
S1C17W18 Technical Manual	413129601	23.2 Recommended Operating Conditions 23.15 Temperature Sensor/ Reference Voltage Generator(TSRVR) Characteristics	23-1 23-18
S1C17W34/W35/W36 Technical Manual	413237901	23.2 Recommended Operating Conditions 23.15 Temperature Sensor/ Reference Voltage Generator(TSRVR) Characteristics	23-1 23-16

(Error)

23.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{PP}	For normal operation	1.2		3.6	V
Capacitor between Vss and V_{PP}	C_{VPP}		–	0.1	–	µF
Capacitor between Vss and VREFA	C_{VREFA}	*6	–	1	–	µF

*1 The C_{V1}–C_{V2} pins can be left open when super economy mode is not used.
*2 The V_{C1}–V_{C4} and C_{P1}–C_{P4} pins can be left open when the LCD driver is not used.

23.15 Temperature Sensor/Reference Voltage Generator (TSRVR) Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{REFA} (2.5 V) output voltage	V_{VO25}	V_{DD} = 2.7 to 3.6 V, I_{load} = 0 µA	2.4	2.5	2.6	V
V_{REFA} (2.0 V) output voltage	V_{VO20}	V_{DD} = 2.2 to 3.6 V, I_{load} = 0 µA	1.9	2.0	2.1	V
V_{REFA} (V_{DD}) output voltage	V_{VODD}	V_{DD} = 1.8 to 3.6 V, I_{load} = 0 µA	V_{DD} - 0.1	V_{DD}	V_{DD} + 0.1	V
V_{REFA} (2.5/2.0 V) operating current	I_{VO1}	V_{DD} = 3.6 V, Ta = 25 °C, I_{load} = 0 µA	25	40	55	µA
V_{REFA} (V_{DD}) operating current	I_{VO2}	V_{DD} = 3.6 V, Ta = 25 °C, I_{load} = 0 µA	–	0.0	0.1	µA
V_{REFA} output voltage stabilization time	t_{VREFA}	C_{VREFA} = 1 µF	–	–	200	µs
Temperature sensor output voltage	V_{TEMP}	V_{DD} = 2.2 to 3.6 V, Ta = 25 °C	1.04	1.07	1.1	V
Temperature sensor output voltage temperature coefficient	ΔV_{TEMP}	V_{DD} = 2.2 to 3.6 V	–	3.6 ± 3%	3.7 ± 6%	mV/°C
Temperature sensor operating current	I_{VTEMP}	V_{DD} = 3.6 V, Ta = 25 °C	10	16	22	µA
Temperature sensor output stabilization time	t_{TEMP}		–	–	200	µs

(Correct)

23.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	For normal operation	1.2		3.6	V
Capacitor between Vss and V_{PP}	C_{VPP}		–	0.1	–	µF
Capacitor between Vss and VREFA	C_{VREFA}	*6	–	0.1	–	µF

*1 The C_{V1}–C_{V2} pins can be left open when super economy mode is not used.
*2 The V_{C1}–V_{C4} and C_{P1}–C_{P4} pins can be left open when the LCD driver is not used.

23.15 Temperature Sensor/Reference Voltage Generator (TSRVR) Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{REFA} (2.5 V) output voltage	V_{VO25}	V_{DD} = 2.7 to 3.6 V, I_{load} = 0 µA	2.4	2.5	2.6	V
V_{REFA} (2.0 V) output voltage	V_{VO20}	V_{DD} = 2.2 to 3.6 V, I_{load} = 0 µA	1.9	2.0	2.1	V
V_{REFA} (V_{DD}) output voltage	V_{VODD}	V_{DD} = 1.8 to 3.6 V, I_{load} = 0 µA	V_{DD} - 0.1	V_{DD}	V_{DD} + 0.1	V
V_{REFA} (2.5/2.0 V) operating current	I_{VO1}	V_{DD} = 3.6 V, Ta = 25 °C, I_{load} = 0 µA	25	40	55	µA
V_{REFA} (V_{DD}) operating current	I_{VO2}	V_{DD} = 3.6 V, Ta = 25 °C, I_{load} = 0 µA	–	0.0	0.1	µA
V_{REFA} output voltage stabilization time	t_{VREFA}	C_{VREFA} = 0.1uF	–	1.5	5	ms
Temperature sensor output voltage	V_{TEMP}	V_{DD} = 2.2 to 3.6 V, Ta = 25 °C	1.04	1.07	1.1	V
Temperature sensor output voltage temperature coefficient	ΔV_{TEMP}	V_{DD} = 2.2 to 3.6 V	–	3.6 ± 3%	3.7 ± 6%	mV/°C
Temperature sensor operating current	I_{VTEMP}	V_{DD} = 3.6 V, Ta = 25 °C	10	16	22	µA
Temperature sensor output stabilization time	t_{TEMP}		–	–	200	µs

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S1C17 Family Technical Manual Errata

ITEM UART (UART) Characteristics

Object manual	Document code	Object item	Page
S7C17W03/W04 Technical Manual	412925001	21.9 UART (UART) Characteristics	21-9
S1C17W13 Technical Manual	413180401	21.9 UART (UART2) Characteristics	21-10
S1C17W14/16 Technical Manual	412910300	22.9 UART (UART) Characteristics	22-9
S1C17W15 Technical Manual	412645702	20.9 UART (UART) Characteristics	20-9
S1C17W18 Technical Manual	413129601	23.9 UART (UART) Characteristics	23-9
S1C17W22/W23 Technical Manual	412690402	23.9 UART (UART) Characteristics	23-9

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(Error)

Unless otherwise specified: V_{DD} = 1.2 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT1}	Normal mode	1.6 to 3.6 V	150	–	230,400	bps
			1.2 to 1.6 V	150	–	57,600	bps
	U_{BRT2}	IrDA mode	1.6 to 3.6 V	150	–	57,600	bps
			1.2 to 1.6 V	150	–	14,400	bps

(Correct)

Unless otherwise specified: V_{DD} = 1.2 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT1}	Normal mode	1.6 to 3.6 V	150	–	460,800	bps
			1.2 to 1.6 V	150	–	57,600	bps
	U_{BRT2}	IrDA mode	1.6 to 3.6 V	150	–	115,200	bps
			1.2 to 1.6 V	150	–	57,600	bps

Others

(Error)

Unless otherwise specified: V_{DD} = 1.2 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT1}	Normal mode	1.6 to 3.6 V	150	–	230,400	bps
			1.2 to 1.6 V	150	–	57,600	bps
	U_{BRT2}	IrDA mode	1.6 to 3.6 V	150	–	57,600	bps
			1.2 to 1.6 V	150	–	14,400	bps

(Correct)

Unless otherwise specified: V_{DD} = 1.2 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT1}	Normal mode	1.6 to 3.6 V	150	–	230,400	bps
			1.2 to 1.6 V	150	–	57,600	bps
	U_{BRT2}	IrDA mode	1.6 to 3.6 V	150	–	115,200	bps
			1.2 to 1.6 V	150	–	57,600	bps

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S1C17 Family Technical Manual Errata

ITEM Appendix A List of Peripheral Circuit Control Registers			
Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	14.4.3 External Voltage Application Mode 2	14-4
S7C17M11 Technical Manual	413393900	17.4.3 External Voltage Application Mode 2	17-4
S1C17W13 Technical Manual	413180401	18.4.3 External Voltage Application Mode 2	18-4
S1C17W14/16 Technical Manual	412910300	18.4.3 External Voltage Application Mode 2	18-4
S1C17W15 Technical Manual	412645702	17.4.3 External Voltage Application Mode 2	17-4
S1C17W18 Technical Manual	413129601	18.4.3 External Voltage Application Mode 2	18-4
S1C17W22/W23 Technical Manual	412690402	18.4.3 External Voltage Application Mode 2	18-4

S1C17W22/W23, S1C17W18 Technical Manual

(Error)

In this mode, one of the LCD drive voltages VC1 to VC4 are applied from outside the IC and other voltages are internally generated. To put LCD24A into external voltage application mode 2, set the LCD24PWR.VCEN bit to 0 to turn the LCD voltage regulator off and the LCD24PWR.BSTEN bit to 1 to turn the LCD voltage booster on.

(Correct)

In this mode, one of the LCD drive voltages VC1 to VC2 are applied from outside the IC and other voltages are internally generated. To put LCD24A into external voltage application mode 2, set the LCD24PWR.VCEN bit to 0 to turn the LCD voltage regulator off and the LCD24PWR.BSTEN bit to 1 to turn the LCD voltage booster on.

S1C17W14/W16, S1C17M01, S7C17M11 Technical Manual

(Error)

In this mode, one of the LCD drive voltages VC1 to VC3 are applied from outside the IC and other voltages are internally generated. To put LCD8B into external voltage application mode 2, set the LCD8PWR.VCEN bit to 0 to turn the LCD voltage regulator off and the LCD8PWR.BSTEN bit to 1 to turn the LCD voltage booster on.

(Correct)

In this mode, one of the LCD drive voltages VC1 to VC2 are applied from outside the IC and other voltages

are internally generated. To put LCD8B into external voltage application mode 2, set the LCD8PWR.VCEN bit to 0 to turn the LCD voltage regulator off and the LCD8PWR.BSTEN bit to 1 to turn the LCD voltage booster on.
S1C17W13 Technical Manual
(Error) In this mode, all the LCD drive voltages VC1 to VC3 are applied from outside the IC. To put LCD4A into external voltage application mode 1, set the LCD4PWR.EXVCSEL bit to 1 and set both the LCD4PWR.VCEN and LCD4PWR.BSTEN bits to 0 to turn both the LCD voltage regulator and LCD voltage booster off.
(Correct) In this mode, all the LCD drive voltages VC1 to VC2 are applied from outside the IC. To put LCD4A into external voltage application mode 1, set the LCD4PWR.EXVCSEL bit to 1 and set both the LCD4PWR.VCEN and LCD4PWR.BSTEN bits to 0 to turn both the LCD voltage regulator and LCD voltage booster off.

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S1C17 Family Technical Manual Errata

ITEM **16bits PWM timer (T16B)**			
Object manual	Document code	Object item	Page
S1C17589 Technical Manual	412959200	16bits PWM timer (T16B)	15-5
S1C17M10 Technical Manul	413180200		16-5
S1C17W03/W04Technical manual	412925001		15-5
S1C17W13 Technical Manual	413180401		15-5
S1C17W14/16Technical Manual	412910300		15-5
S1C17W15Technical Manual	412645702		15-5
S1C17W18Technical Manual	413129601		15-5
S1C17W22/W23 Technical Manual	412690402		15-5
S1C17W34/W35/W36 Technical Manual	413237901		15-5
S7C17M11 Technical Manual	413393900		15-5

1.1 Features

(Error)

MAX counter data register

The MAX counter data register (T16B*n*MC.MC[15:0] bits) is used to set the maximum value of the counter (hereafter referred to as MAX value). This setting limits the count range to 0x0000–MAX value and determines the count and interrupt cycles. When the counter is set to repeat mode, the MAX value can be rewritten in the procedure shown below even if the counter is running.

1. Check to see if the T16B*n*CTL.MAXBSY bit is set to 0.
2. Write the MAX value to the T16B*n*MC.MC[15:0] bits.

(Correct)

Add note statement (underlined).

MAX counter data register

The MAX counter data register (T16B*n*MC.MC[15:0] bits) is used to set the maximum value of the counter (hereafter referred to as MAX value). This setting limits the count range to 0x0000–MAX value and determines the count and interrupt cycles. When the counter is set to repeat mode, the MAX value can be rewritten in the procedure shown below even if the counter is running.

1. Check to see if the T16B*n*CTL.MAXBSY bit is set to 0.
2. Write the MAX value to the T16B*n*MC.MC[15:0] bits.

Note: When rewriting the MAX value, the new MAX value should be written after the counter has been reset to the previously set MAX value.

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errata_c17w18_7

S1C17 Family Technical Manual Errata

ITEM **VDD operating voltage for Flash programming.**

Object manual	Document code	Object item	Page
S1C17W13 Technical Manual	413180401	1.1 Features 4.3.3 Flash Programming 21.2 Recommended Operating Conditions 21.6 Flash Memory Characteristics	1-2 4-3 21-1 21-7
S1C17W18 Technical Manual	413129601	1.1 Features 4.3.3 Flash Programming 23.2 Recommended Operating Conditions 23.6 Flash Memory Characteristics	1-2 4-3 23-1 23-7
S1C17W34/W35/W36 Technical Manual	413237901	1.1 Features 4.3.3 Flash Programming 23.2 Recommended Operating Conditions 23.6 Flash Memory Characteristics	1-2 4-3 23-1 23-7
S1C17M10 Technical Manual	413180200	1.1 Features 4.3.3 Flash Programming 19.2 Recommended Operating Conditions 19.6 Flash Memory Characteristics	1-2 4-3 19-1 19-7

1.1 Features : S1C17W13

(Error)

Power supply voltage	
VDD operating voltage for Flash programming	1.8 to 3.6 V (VPP = 7.5 V external power supply is required.)

(Correct)

Power supply voltage	
VDD operating voltage for Flash programming	2.4 to 3.6 V (VPP = 7.5 V external power supply is required.)

1.1 Features : S1C17W18, S1C17W34/W35/W36

(Error)

Power supply voltage	
VDD operating voltage for Flash programming	1.8 to 3.6 V (VPP = 7.5 V external power supply is required.) 2.7 to 3.6 V (When VPP is generated internally)

(Correct)

Power supply voltage	
VDD operating voltage for Flash programming	2.4 to 3.6 V (VPP = 7.5 V external power supply is required.) 2.7 to 3.6 V (When VPP is generated internally)

1.1 Features : S1C17M10

(Error)

Power supply voltage	
VDD operating voltage for Flash programming	1.8 to 5.5 V (VPP = 7.5 V external power supply is required.) 2.7 to 5.5 V (When VPP is generated internally)

(Correct)

Power supply voltage	
VDD operating voltage for Flash programming	2.4 to 5.5 V (VPP = 7.5 V external power supply is required.) 2.7 to 5.5 V (When VPP is generated internally)

4.3.3 Flash Programming : S1C17W13

(Error)

Note: The Flash programming requires a 1.8 V or higher VDD voltage.

(Correct)

Note: The Flash programming requires a 2.4 V or higher VDD voltage.

4.3.3 Flash Programming : S1C17W18, S1C17W34/W35/W36

(Error)

Notes: • The Flash programming requires a 1.8 V or higher VDD voltage when the VPP voltage is supplied externally.

(Correct)

Notes: • The Flash programming requires a 2.4 V or higher VDD voltage when the VPP voltage is supplied externally.

4.3.3 Flash Programming : S1C17M10

(Error)

Notes: • The Flash programming requires a VDD voltage within 2.2 V to 5.5 V when the VPP voltage is generated internally.

(Correct)

Notes: • The Flash programming requires a 2.4 V or higher VDD voltage when the VPP voltage is supplied externally.
• The Flash programming requires a 2.7 V or higher VDD voltage when the VPP voltage is generated internally.

21.2 Recommended Operating Conditions : S1C17W13

(Error)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	VDD	For Flash programming	1.8	–	3.6	V

(Correct)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	VDD	For Flash programming	2.4	–	3.6	V

23.2 Recommended Operating Conditions : S1C17W18, S1C17W34/W35/W36

(Error)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power supply voltage	VDD	For Flash programming	When VPP is supplied externally	1.8	–	3.6	V
			When VPP is generated internally	2.7	–	3.6	V

(Correct)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power supply voltage	VDD	For Flash programming	When VPP is supplied externally	2.4	–	3.6	V
			When VPP is generated internally	2.7	–	3.6	V

19.2 Recommended Operating Conditions : S1C17M10

(Error)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power supply voltage	VDD	For Flash programming	When VPP is supplied externally	1.8	–	5.5	V
			When VPP is generated internally	2.7	–	5.5	V

(Correct)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power supply voltage	VDD	For Flash programming	When VPP is supplied externally	2.4	–	5.5	V
			When VPP is generated internally	2.7	–	5.5	V

21.6 Flash Memory Characteristics : S1C17W13 23.6 Flash Memory Characteristics : S1C17W18, S1C17W34/W35/W36
(Error) Unless otherwise specified: VDD = 1.8 to 3.6 V, VSS = 0 V, Ta = -40 to 85 °C
(Correct) Unless otherwise specified: VDD = 2.4 to 3.6 V, VSS = 0 V, Ta = -40 to 85 °C
19.6 Flash Memory Characteristics : S1C17M10
(Error) Unless otherwise specified: VDD = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to 85 °C
(Correct) Unless otherwise specified: VDD = 2.4 to 5.5 V, VSS = 0 V, Ta = -40 to 85 °C

Feb/20/2017

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S1C17 Family Technical Manual Errata

ITEM **Electrical Characteristics**

Object manual	Document code	Object item	Page
S1C17W18 Technical Manual	413129601	23.15 Temperature Sensor/Reference Voltage Generator(TSRVR) Characteristics	23-18
S1C17W34/W35/W36 Technical Manual	413237901	23.15 Temperature Sensor/Reference Voltage Generator(TSRVR) Characteristics	23-16

(Error)

S1C17W18

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VREFA (2.5 V) output voltage	VVO25	VDD = 2.7 to 3.6 V, Iload = 0 µA	2.4	2.5	2.6	V
VREFA (2.0 V) output voltage	VVO20	VDD = 2.2 to 3.6 V, Iload = 0 µA	1.9	2.0	2.1	V
VREFA (VDD) output voltage	VVODD	VDD = 1.8 to 3.6 V, Iload = 0 µA	VDD - 0.1	VDD	VDD + 0.1	V
VREFA (2.5/2.0 V) operating current	IVO1	VDD = 3.6 V, Ta = 25 °C, Iload = 0 µA	25	40	55	µA
VREFA (VDD) operating current	IVO2	VDD = 3.6 V, Ta = 25 °C, Iload = 0 µA	–	0.0	0.1	µA
VREFA output voltage stabilization time	tVREFA	CVREFA = 1 µF	–	–	200	µs
Temperature sensor output voltage	VTEMP	VDD = 2.2 to 3.6 V, Ta = 25 °C	1.04	1.07	1.1	V
Temperature sensor output voltage temperature coefficient	ΔVTEMP	VDD = 2.2 to 3.6 V	–	3.6 ± 3%	3.7 ± 6%	mV/°C
Temperature sensor operating current	IVTEMP	VDD = 3.6 V, Ta = 25 °C	10	16	22	µA
Temperature sensor output stabilization time	tTEMP		–	–	200	µs

S1C17W34/W35/W36

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VREFA (2.5 V) output voltage	VVO25	VDD = 2.7 to 3.6 V, Iload = 0.5 mA	2.4	2.5	2.6	V
VREFA (2.0 V) output voltage	VVO20	VDD = 2.2 to 3.6 V, Iload = 0.1 mA	1.9	2.0	2.1	V
VREFA (VDD) output voltage	VVODD	VDD = 1.8 to 3.6 V, Iload = 0.3 mA	VDD - 0.1	VDD	VDD + 0.1	V
VREFA (2.5/2.0 V) operating current	IVO1	VDD = 3.6 V, Ta = 25 °C, Iload = 0 µA	25	40	55	µA
VREFA (VDD) operating current	IVO2	VDD = 3.6 V, Ta = 25 °C, Iload = 0 µA	–	0.0	0.1	µA
VREFA output voltage stabilization time	tVREFA		–	–	200	µs
Temperature sensor output voltage	VTEMP	VDD = 2.2 to 3.6 V, Ta = 25 °C	1.04	1.07	1.1	V
Temperature sensor output voltage temperature coefficient	ΔVTEMP	VDD = 2.2 to 3.6 V	–	3.6	3.7 ± 6%	mV/°C
Temperature sensor operating current	IVTEMP	VDD = 3.6 V, Ta = 25 °C	10	16	22	µA
Temperature sensor output stabilization time	tTEMP		–	–	200	µs

(Correct)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VREFA (2.5 V) output voltage	VVO25	VDD = 2.7 to 3.6 V	2.4	2.5	2.6	V
VREFA (2.0 V) output voltage	VVO20	VDD = 2.2 to 3.6 V	1.9	2.0	2.1	V
VREFA (VDD) output voltage	VVODD	VDD = 1.8 to 3.6 V	VDD - 0.1	VDD	VDD + 0.1	V
VREFA (2.5/2.0 V) operating current	IVO1	VDD = 3.6 V, Ta = 25 °C	25	40	55	µA
VREFA (VDD) operating current	IVO2	VDD = 3.6 V, Ta = 25 °C	–	0.0	0.1	µA
VREFA output voltage stabilization time	tVREFA	CVREFA = 1 µF	–	5	50	ms
Temperature sensor output voltage	VTEMP	VDD = 2.2 to 3.6 V, Ta = 25 °C	1.04	1.07	1.1	V
Temperature sensor output voltage temperature coefficient	ΔVTEMP	VDD = 2.2 to 3.6 V	–	3.6 ± 3%	3.7 ± 6%	mV/°C
Temperature sensor operating current	IVTEMP	VDD = 3.6 V, Ta = 25 °C	10	16	22	µA
Temperature sensor output stabilization time	tTEMP		–	–	200	µs

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S1C17 Family Technical Manual Errata

ITEM **DCLK pin precautions**			
Object manual	Document code	Object item	Page
S1C17W03/W04 Technical Manual	412925001	3.3.3 List of debugger input/output pins	3-3
S1C17W13 Technical Manual	413180401	3.3.3 List of debugger input/output pins	3-3
S1C17W14/W16 Technical Manual	412910300	3.3.3 List of debugger input/output pins	3-3
S1C17W15 Technical Manual	412645702	3.3.3 List of debugger input/output pins	3-3
S1C17W18 Technical Manual	413129601	3.3.3 List of debugger input/output pins	3-3
S1C17W22/W23 Technical Manual	412690402	3.3.3 List of debugger input/output pins	3-3
S1C17W34/W35/W36 Technical Manual	413237901	3.3.3 List of debugger input/output pins	3-3
S1C17M01 Technical Manual	412361701	3.3.3 List of debugger input/output pins	3-3
S1C17M10 Technical Manual	413180200	3.3.3 List of debugger input/output pins	3-3
S1C17589 Technical Manual	412959200	3.3.3 List of debugger input/output pins	3-3

(Error)

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the “I/O Ports” chapter.

(Correct)

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the “I/O Ports” chapter.

Note: The DCLK pin can’t drive by high level input from external. (E.g. The pin is done pull-up etc.) Also, the DCLK pin and the other general purpose I/O pins can’t connect by a short. Because in both cases, it has possibility that the IC can’t work normally by the effect of unstable I/O at power-on.

S1C17 Family Technical Manual Errata

ITEM **I²C(I2C)**			
Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	8.6 Control Registers	8-6
S1C17F13 Technical Manual	412486301	8.6 Control Registers	8-6
S1C17W22/W23 Technical Manual	412690402	9.6 Control Registers	9-6
S1C17W15 Technical Manual	412645702	9.6 Control Registers	9-6
S1C17589 Technical Manual	412959200	9.6 Control Registers	9-6
S1C17W14/W16 Technical Manual	412910300	9.6 Control Registers	9-6
S1C17W03/W04 Technical Manual	412925001	9.6 Control Registers	9-6
S1C17W18 Technical Manual	413129601	9.6 Control Registers	9-6
S1C17M10 Technical Manual	413180200	9.6 Control Registers	9-6
S1C17W13 Technical Manual	413180401	9.6 Control Registers	9-6
S1C17W34/W35/W36 Technical Manual	413237901	9.6 Control Registers	9-6

(Error)

14.4.3 Data Reception in Master Mode

A data receiving procedure in master mode and the I2C Ch.n operations are shown below. Figures 14.4.3.1 and 14.4.3.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1. Issue a START condition by setting the I2CnCTL.TXSTART bit to 1.
2. Wait for a transmit buffer empty interrupt (I2CnINTF.TBEIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).
   Clear the I2CnINTF.STARTIF bit by writing 1 after the interrupt has occurred.
3. Write the 7-bit slave address to the I2CnTXD.TXD[7:1] bits and 1 that represents READ as the data transfer direction to the I2CnTXD.TXD0 bit.
4. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or a NACK reception interrupt (I2CnINTF.NACKIF bit=1) generated when a NACK is received.
   i. Go to Step 5 when a receive buffer full interrupt has occurred.
   ii. Clear the I2CnINTF.NACKIF bit and issue a STOP condition by setting the I2CnCTL.TXSTOP bit to 1 when a NACK reception interrupt has occurred. Then go to Step 8 or Step 1 if making a retry.
5. Perform one of the operations below when the last or next-to-last data is received.
   i. When the next-to-last data is received, write 1 to the I2CnCTL.TXNACK bit to send a NACK after the last data is received, and then go to Step 6.
   ii. When the last data is received, read the received data from the I2CnRXD register and set the

I2CnCTL.TXSTOP to 1 to generate a STOP condition. Then go to Step 8.

6. Read the received data from the I2CnRXD register.
7. Repeat Steps 4 to 6 until the end of data reception.
8. Wait for a STOP condition interrupt (I2CnINTF.STOPIF bit=1).
   Clear the I2CnINTF.STOPIF bit by writing 1 after the interrupt has occurred.

Data receiving operations

(abbrev.)

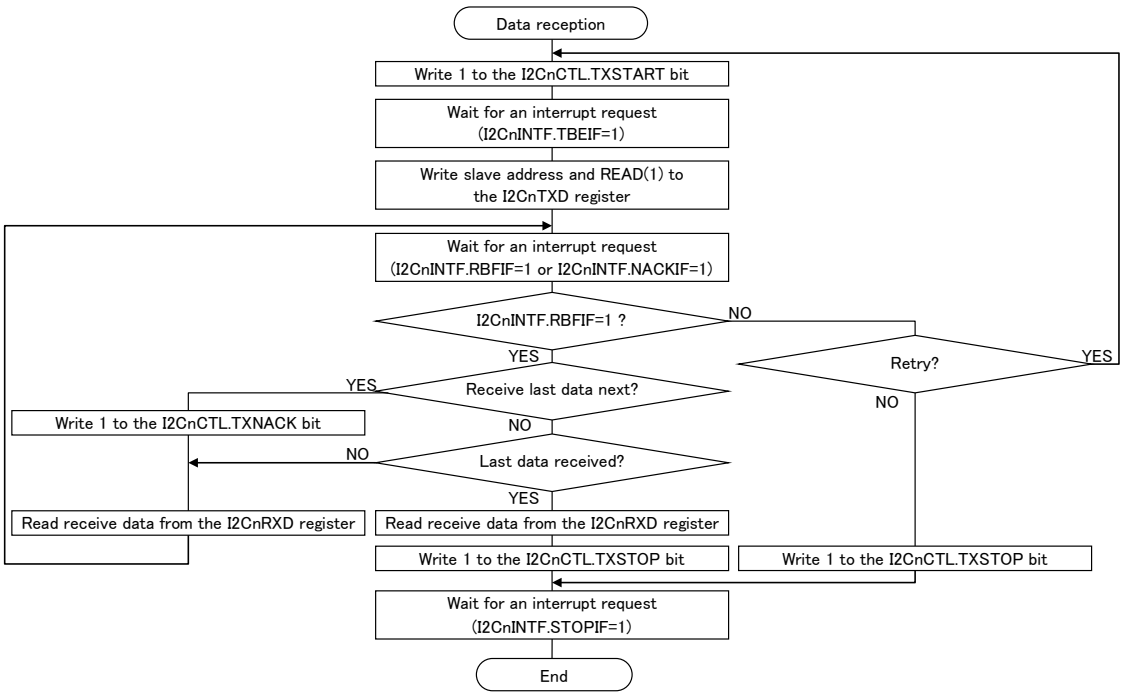

Figure 14.4.3.2 Master Mode Data Reception Flowchart

14.4.6 Data Reception in Slave Mode

A data receiving procedure in slave mode and the I2C Ch.n operations are shown below. Figures 14.4.6.1 and 14.4.6.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1. Wait for a START condition interrupt (I2CnINTF.STARTIF bit=1).
2. Check to see if the I2CnINTF.TR bit=0 (reception mode).
   (Start a data sending procedure if I2CnINTF.TR bit=1.)
3. Clear the I2CnINTF.STARTIF bit by writing 1.
4. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or an end of transfer interrupt (I2CnINTF.BYTEENDIF bit=1).
   Clear the I2CnINTF.BYTEENDIF bit by writing 1 after the interrupt has occurred.
5. If the next receive data is the last one, write 1 to the I2CnCTL.TXNACK bit to send a NACK after it is received.

6. Read the received data from the I2CnRXD register.
7. Repeat Steps 4 to 6 until the end of data reception.
8. Wait for a STOP condition interrupt (I2CnINTF.STOPIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).
   i. Go to Step 9 when a STOP condition interrupt has occurred.
   ii. Go to Step 2 when a START condition interrupt has occurred.
9. Clear the I2CnINTF.STOPIF bit and then terminate data receiving operations.

Data receiving operations

(abbrev.)

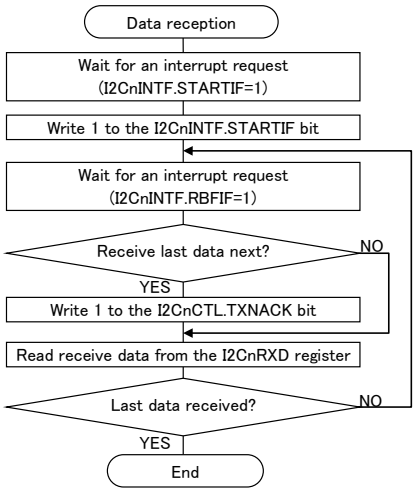

Figure 14.4.6.2 Slave Mode Data Reception Flowchart

(Correct)

14.4.3 Data Reception in Master Mode

A data receiving procedure in master mode and the I2C Ch.n operations are shown below. Figures 14.4.3.1 and 14.4.3.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1.When a one-byte reception, write 1 to the I2CnCTL.TXNACK bit.
2. Issue a START condition by setting the I2CnCTL.TXSTART bit to 1.
3. Wait for a transmit buffer empty interrupt (I2CnINTF.TBEIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).
   Clear the I2CnINTF.STARTIF bit by writing 1 after the interrupt has occurred.
4. Write the 7-bit slave address to the I2CnTXD.TXD[7:1] bits and 1 that represents READ as the data transfer direction to the I2CnTXD.TXD0 bit.
5. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or a NACK reception interrupt (I2CnINTF.NACKIF bit=1) generated when a NACK is received.

i. Go to Step 6 when a receive buffer full interrupt has occurred.

ii. Clear the I2CnINTF.NACKIF bit and issue a STOP condition by setting the I2CnCTL.TXSTOP bit to 1 when a NACK reception interrupt has occurred. Then go to Step 9 or Step 2 if making a retry.

6. Perform one of the operations below when the last or next-to-last data is received.

i. When the next-to-last data is received, write 1 to the I2CnCTL.TXNACK bit to send a NACK after the last data is received, and then go to Step 7.

ii. When the last data is received, read the received data from the I2CnRXD register and set the I2CnCTL.TXSTOP to 1 to generate a STOP condition. Then go to Step 9.

7. Read the received data from the I2CnRXD register.

8. Repeat Steps 5 to 7 until the end of data reception.

9. Wait for a STOP condition interrupt (I2CnINTF.STOPIF bit=1).
Clear the I2CnINTF.STOPIF bit by writing 1 after the interrupt has occurred.

Data receiving operations

(abbrev.)

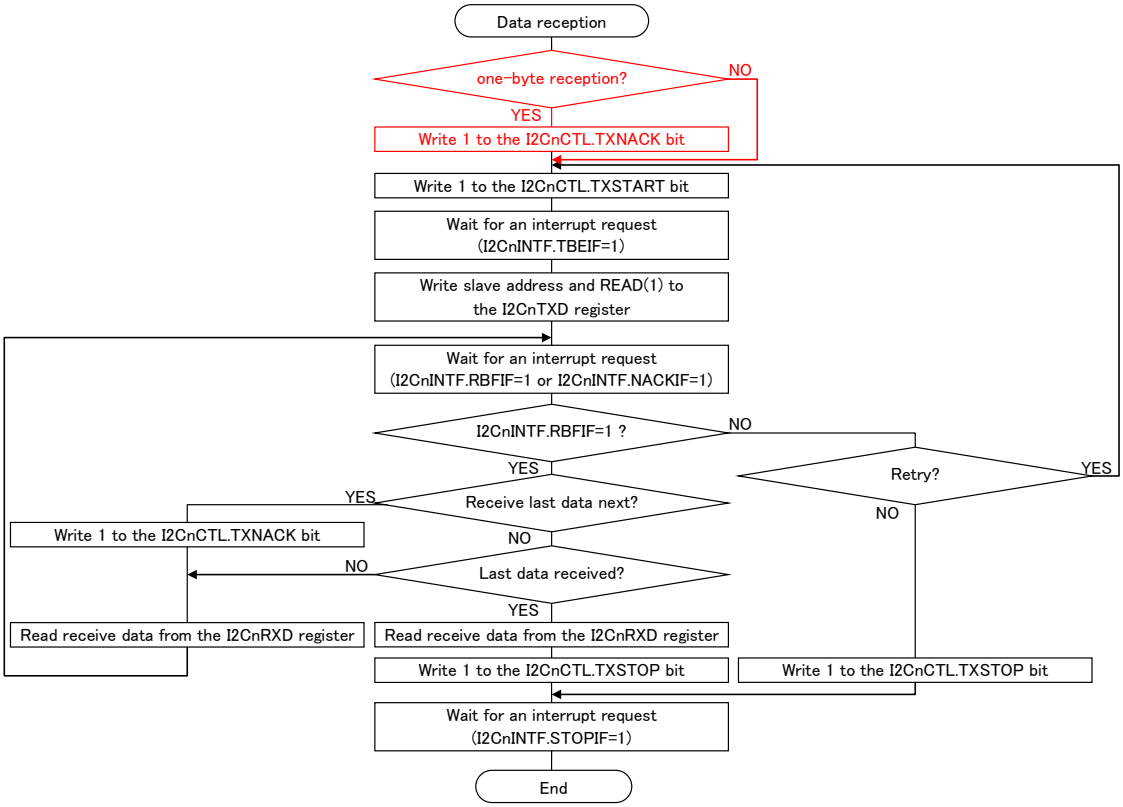

Figure 14.4.3.2 Master Mode Data Reception Flowchart

14.4.6 Data Reception in Slave Mode

A data receiving procedure in slave mode and the I2C Ch.n operations are shown below. Figures 14.4.6.1 and 14.4.6.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1.When a one-byte reception, write 1 to the I2CnCTL.TXNACK bit.

2. Wait for a START condition interrupt (I2CnINTF.STARTIF bit=1).

3. Check to see if the I2CnINTF.TR bit=0 (reception mode).
   (Start a data sending procedure if I2CnINTF.TR bit=1.)

4. Clear the I2CnINTF.STARTIF bit by writing 1.

5. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or an end of transfer interrupt (I2CnINTF.BYTEENDIF bit=1).
   Clear the I2CnINTF.BYTEENDIF bit by writing 1 after the interrupt has occurred.

6. If the next receive data is the last one, write 1 to the I2CnCTL.TXNACK bit to send a NACK after it is received.

7. Read the received data from the I2CnRXD register.

8. Repeat Steps 5 to 7 until the end of data reception.

9. Wait for a STOP condition interrupt (I2CnINTF.STOPIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).
   i. Go to Step 10 when a STOP condition interrupt has occurred.
   ii. Go to Step 3 when a START condition interrupt has occurred.

10. Clear the I2CnINTF.STOPIF bit and then terminate data receiving operations.

Data receiving operations

(abbrev.)

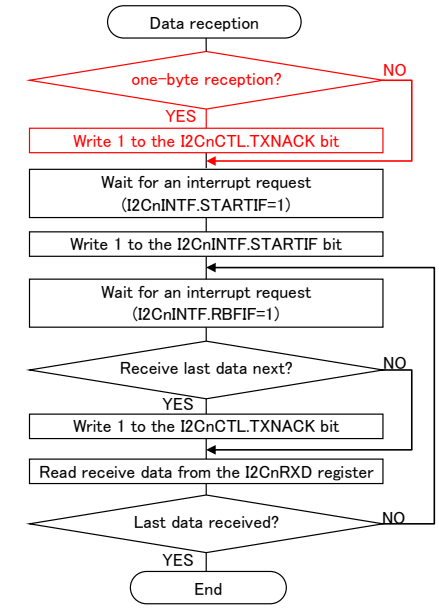

Figure 14.4.6.2 Slave Mode Data Reception Flowchart

Aug/03/2016

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S1C17 Family Technical Manual Errata

ITEM **Real-Time Clock (RTCA)**

Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	8.6 Control Registers	8-6
S1C17F13 Technical Manual	412486301	8.6 Control Registers	8-6
S1C17W22/W23 Technical Manual	412690402	9.6 Control Registers	9-6
S1C17W15 Technical Manual	412645702	9.6 Control Registers	9-6
S1C17589 Technical Manual	412959200	9.6 Control Registers	9-6
S1C17W14/W16 Technical Manual	412910300	9.6 Control Registers	9-6
S1C17W03/W04 Technical Manual	412925001	9.6 Control Registers	9-6
S1C17W18 Technical Manual	413129601	9.6 Control Registers	9-6
S1C17M10 Technical Manual	413180200	9.6 Control Registers	9-6
S1C17W13 Technical Manual	413180401	9.6 Control Registers	9-6
S1C17W34/W35/W36 Technical Manual	413237901	9.6 Control Registers	9-6

(Error)

Bits14–8 RTCTRM[6:0]

Write the correction value for adjusting the 1 Hz frequency to these bits to execute theoretical regulation.For a calculation method of correction value, refer to “Theoretical Regulation Function.”

Note: When the RTCCTL.RTCTRMBSY bit = 1, the RTCCTL.RTCTRM[6:0] bits cannot be rewritten.

(Correct)

Bits14–8 RTCTRM[6:0]

Write the correction value for adjusting the 1 Hz frequency to these bits to execute theoretical regulation.For a calculation method of correction value, refer to “Theoretical Regulation Function.”

Notes: ・When the RTCCTL.RTCTRMBSY bit = 1, the RTCCTL.RTCTRM[6:0] bits cannot be rewritten.

・When 0x00 is written to the RTCCTL.RTCTRM[6:0] bits, the RTCCTL.RTCTRMBSY bit goes 1, but the time-of-day clock is not corrected.

Aug/03/2016

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S1C17 Family Technical Manual Errata

ITEM **Watchdog Timer (WDT)**

Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	7.4 Control Registers	7-3~4
S1C17F13 Technical Manual	412486301	7.4 Control Registers	7-3~4
S1C17W22/W23 Technical Manual	412690402	8.4 Control Registers	8-3~4
S1C17W15 Technical Manual	412645702	8.4 Control Registers	8-3~4
S1C17589 Technical Manual	412959200	8.4 Control Registers	8-3~4
S1C17W14/W16 Technical Manual	412910300	8.4 Control Registers	8-3~4
S1C17W03/W04 Technical Manual	412925001	8.4 Control Registers	8-3~4
S1C17W18 Technical Manual	413129601	8.4 Control Registers	8-3~4

(Error)

Bits 3–0 WDTRUN[3:0]

These bits control WDT to run and stop.

0xa (R/WP): Stop

Values other than 0xa (R/WP): Run

Always 0x0 is read if a value other than 0xa is written.

Since a reset may be generated immediately after running depending on the counter value, WDT should also be reset concurrently when running WDT.

(Correct)

Bits 3–0 WDTRUN[3:0]

These bits control WDT to run and stop.

0xa (WP): Stop

Values other than 0xa (WP): Run

0xa (R): Stopping

0x0 (R): Running

Always 0x0 is read if a value other than 0xa is written.

Since a reset may be generated immediately after running depending on the counter value, WDT should also be reset concurrently when running WDT.

June/2/2016

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S1C17 Family Technical Manual Errata

ITEM **12-bit A/D Converter (ADC12A)**			
Object manual	Document code	Object item	Page
S1C17W18 Technical Manual	413129601	20.6 Control Register AP.A List of Peripheral Circuit Control Registers	20-6, 20-7 AP-A-29

20.6 Control Register

(Error)

ADC12A Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC12_*n*CTL	15	–	0	–	R	–
	14–12	ADSTAT[2:0]	0x0	H0	R	
	11	–	0	–	R	
	10	BSYSTAT	1	H0	R	
	9–8	–	0x0	–	R	
	7–2	–	0x00	–	R	
	1	ADST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bit10 BSYSTAT

This bit indicates whether the ADC12A is executing A/D conversion or not.

1 (R/W): A/D converting

0 (R/W): Idle

Note: The ADC12_nCTL.BSYSTAT bit is cleared to 0 when the clock is supplied to ADC12A by setting the ADC12_nCTL.MODEN bit to 1.

(Correct)

ADC12A Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC12_*n*CTL	15	–	0	–	R	–
	14–12	ADSTAT[2:0]	0x0	H0	R	
	11	–	0	–	R	
	10	BSYSTAT	0	H0	R	
	9–8	–	0x0	–	R	
	7–2	–	0x00	–	R	
	1	ADST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bit10 BSYSTAT

This bit indicates whether the ADC12A is executing A/D conversion or not.

1 (R/W): A/D converting

0 (R/W): Idle

~~Note: The ADC12_nCTL.BSYSTAT bit is cleared to 0 when the clock is supplied to ADC12A by setting the ADC12_nCTL.MODEN bit to 1.~~

Appendix A. List of Peripheral Circuit Control Registers

(Error)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54a2	ADC12_0CTL (ADC12A Ch.0 Control Register)	15	–	0	–	R	–
		14–12	ADSTAT[2:0]	0x0	H0	R	
		11	–	0	–	R	
		10	BSYSTAT	1	H0	R	
		9–8	–	0x0	–	R	
		7–2	–	0x00	–	R	
		1	ADST	0	H0	R/W	
		0	MODEN	0	H0	R/W	

(Correct)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54a2	ADC12_0CTL (ADC12A Ch.0 Control Register)	15	–	0	–	R	–
		14–12	ADSTAT[2:0]	0x0	H0	R	
		11	–	0	–	R	
		10	BSYSTAT	0	H0	R	
		9–8	–	0x0	–	R	
		7–2	–	0x00	–	R	
		1	ADST	0	H0	R/W	
		0	MODEN	0	H0	R/W	